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CERTIFICATION OF TRANSLATION

SIR:

I, the undersigned, Toyoaki SATOH, of c/o KOSHIBA & PARTNERS, 3F Kioi-cho hills, 3-32 Kioi-cho, Chiyoda-ku, Tokyo 102-0094 JAPAN, hereby declare that I am well familiar, both with the English and Japanese languages, and I have prepared the attached English translation of Japanese text attached to Patent Application No. Heisei 11-182445 filed in Japan on 28th June 1999, and that the English translation is a true, faithful and exact translation of the corresponding Japanese language document.

I further declare that I am aware that willful false statements and the like on this Certification of Translation are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon. Any statements in this Certification of Translation made of my own knowledge are true and all statements made on information and belief are believed to be true.

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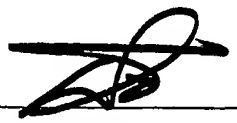

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This is to certify that the annexed is a true copy of the following application as filed with this office.

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[Title of the Invention] STANDARD CELL, STANDARD CELL ARRAY, AND SYSTEM AND METHOD FOR PLACING AND ROUTING STANDARD CELLS

[Claims]

[Claim 1] A standard cell characterized in that it comprises a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal.

[Claim 2] A standard cell comprising a function circuit including at least one P-channel transistor and at least one N-channel transistor; a first power supply terminal for supplying a first power supply voltage to said at least one P-channel transistor, a second power supply terminal for supplying a second power supply voltage to said at least one N-channel transistor, and an input terminal and an output terminal for said function circuit, characterized in that said first power supply terminal is provided at a P-type diffused layer of said at least one P-channel transistor supplied with said first power supply voltage, and said second power supply terminal is provided at an N-type diffused layer of said at least one N-channel transistor supplied with said second power supply voltage, and in that said input terminal and said output terminal for said function circuit are constituted of a first level metal

[Claim 3] A standard cell array characterized in that a plurality of standard cells as claimed in Claim 1 or 2 are located in such a manner that respective well boundary lines within said standard cells are aligned on one straight line, and a substrate contact cell for connecting a first power supply voltage and a second power supply voltage to said semiconductor substrate and a well formed in said semiconductor substrate, respectively, is inserted

into said standard cell array at predetermined intervals, at least one for a predetermined number of standard cells.

[Claim 4] A standard cell placement and routing processing system characterized in that it comprises a library file which stores information of various standard cells as claimed in Claim 1 or 2, a circuit connection information file which stores circuit connection information of an LSI to be developed, a constraint information file which stores constraint information concerning the placement and the routing, a parameter file which stores parameter information including a power supply voltage and an operating frequency of said LSI to be developed and a sheet resistance of said diffused layer, a placement and routing system for executing the placement and the routing of said standard cells by utilizing information from said library file, said circuit connection information file and said parameter file, and an input/output and display apparatus for displaying a history and a result of the placement and the routing and for externally inputting a control command to control said placement and routing system.

[Claim 5] A standard cell placement and routing method executed by using the standard cell placement and routing processing system as claimed in Claim 4, characterized in that the method comprises:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and locating the read-out standard cells into a plurality of standard cell arrays, each of said plurality of standard cell arrays including at least one substrate contact cell inserted for every a predetermined number of standards cells, and said standard cells included in each of said plurality of standard cell arrays

being arranged in such a manner that respective well boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a third step of routing signal lines between the standard cells included in said standard cell array, in accordance with said circuit connection information;

a fourth step of extracting a contour of a wiring area of said signal lines within said standard cell array, and placing a power supply line at the outside of said wiring area;

a fifth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said diffused layer within said standard cell in said standard cell array, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then, forming a contact hole at an overlapping portion between said power supply line and said extended power supply line of said diffused layer;

a sixth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a seventh step of re-routing said signal lines between said standard cells when it is discriminated in said sixth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fourth step; and

an eighth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays when it is discriminated in said sixth step that the resistance of said power supply

line of said diffused layer is not greater than said predetermined resistance value.

[Claim 6] A method claimed in Claim 5 characterized in that said second step includes:

a first sub-step of reading out from said cell library file, said standard cells corresponding to the read-out circuit connection information, and locating said read-out standard cells into a plurality of standard cell arrays in such a manner that respective well boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a second sub-step of inserting said at least one substrate contact cell for every a predetermined number of standards cells in each standard cell array, to complete said plurality of standard cell arrays;

a third sub-step of calculating a power supply line width on the basis of information including the number of the standard cells and the kinds of the standard cells included said standard cell array, said power supply voltage, and said operating frequency;

a fourth sub-step of calculating the width of a routing channel required from said power supply line width, the number of signal lines, and signal paths; and

a fifth sub-step of discriminating whether or not the routing is possible, with reference to a chip size stored in said constraint information file, and returning to said first sub-step when the routing is not possible, and on the other hand, completing said second step when the routing is possible.

[Claim 7] A method claimed in Claim 5 characterized in that said fifth step includes:

a first sub-step of extracting said power supply terminals of said standard cells included in said standard cell array;

a second sub-step of discriminating whether or not the extracted power supply terminal overlaps said power supply line;

a third sub-step of extending said power supply line of said diffused layer from said extracted power supply terminal to said power supply line when said extracted power supply terminal does not overlap said power supply line, so that said extended power supply line of said diffused layer overlaps said power supply line; and

a fourth sub-step of forming a contact hole at an overlapping portion between said extracted power supply terminal and said power supply line when it is discriminated in said second sub-step that said extracted power supply terminal overlaps said power supply line, or alternatively at an overlapping portion between said power supply line and said extended power supply line of said diffused layer when it is discriminated in said second sub-step that said extracted power supply terminal does not overlap said power supply line.

[Claim 8] A method claimed in Claim 5 characterized in that said seventh step includes:

a first sub-step of detecting a signal line which becomes a hindrance in reducing the resistance of said power supply line formed of said diffused layer to not greater than said predetermined resistance value;

a second sub-step of removing said signal line which becomes said hindrance, and providing a through-hole for connecting between said first level metal and a second level metal at an end position to which the removed signal line was connected; and

a third sub-step of discriminating whether or not the resistance of said power supply line formed of said diffused layer shortened as the result

of the removal of said signal line is not greater than said predetermined resistance value, and returning to said first sub-step when the resistance is greater than said predetermined resistance value, or alternatively completing said seventh step when the resistance is not greater than said predetermined resistance value.

[Claim 9] A standard cell placement and routing method executed by using the standard cell placement and routing processing system as claimed in Claim 4, characterized in that the method comprises:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and provisionally locating the read-out standard cells into a plurality of provisional standard cell arrays;

a third step of dividing said provisional standard cell array into a plurality of cell groups each including not greater than a predetermined number of standard cells which are located adjacent to one another;

a fourth step of selecting one cell group to be processed, from said plurality of cell groups;

a fifth step of routing signal lines between said standard cells within said one selected cell group;

a sixth step of extracting a contour of a wiring area of said signal lines within said one selected cell group, to register a power supply line inhibit area in said constraint information file;

a seventh step of placing a power supply line along the outside of said power supply line inhibit area within said one selected cell group;

an eighth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said

diffused layer within said standard cell in said one selected cell group, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then, forming a contact hole at an overlapping portion between said power supply line and said power supply line of said diffused layer;

a ninth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a tenth step of re-routing said signal lines between said standard cells when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fifth step;

an eleventh step of discriminating whether or not the processing for all the cell groups has been completed, when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is not greater than said predetermined resistance value, and then, returning to said fourth step when the processing for all the cell groups has not yet been completed;

a twelfth step of replacing said provisional standard cell array composed of the provisionally located standard cells, with corresponding cell groups processed above, when it is discriminated in said eleventh step that the processing for all the cell groups has been completed;

a thirteenth step of interconnecting respective power supply lines of said cell groups processed above to form a power supply line for said standard cell array; and

a fourteenth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays.

[Detailed Description of the Invention]

[0001]

[Industrial field to which Invention belongs]

The present invention relates to a standard cell formed on a semiconductor substrate, a standard cell array formed on a semiconductor substrate, and a placing and routing system and a placing and routing method of standard cells.

[0002]

[Prior art]

As a layout design technology for realizing a LSI (large scale integrated circuit) on a semiconductor substrate with a high integration density for a short period of time, a standard cell type LSI design technology is widely utilized, in which small unitary circuits such as an inverter and an NAND gate are previously prepared as standard cells, and those standard cells are placed in the form of an array and interconnected to form an LSI.

[0003]

Fig. 18(a) is a layout diagram of a standard cell type LSI. A plurality of cell arrays are placed, each of the cell arrays being formed of a plurality of function cells 106 having the same width (height in the drawing) and placed in the form of an array. A routing channel 1801 is reserved between each pair of adjacent cell arrays. In the routing channel 1801, there are located an inter-cell connection 1802 for interconnecting between cells included in the same cell array, and an inter-array connection 1803 for interconnecting between cells which are included in different cell arrays, respectively.

[0004]

Fig. 18(b) is a pattern diagram of the inside of one typical standard cell. In a function cell 106a having an inverter function, the reference number 111 designates an N-well, and the reference number 112 indicates a P-type diffused layer. The reference number 113 shows an N-type diffused layer, and the reference number 114 denotes a polysilicon. The reference number 115 designates a contact hole between the P-type or N-type diffused layer and a first level metal. The reference number 116 indicates a contact hole between the polysilicon and the first level metal. The reference number 117 shows the first level metal. The reference number 120 denotes a VDD power supply line formed of the first level metal. The reference number 121 designates a VSS power supply line formed of the first level metal. In the N-well 111, a P-channel MOS transistor having a source and a drain formed of the P-type diffused layer 112 is formed. In a P-type substrate region at the outside of the N-well, an N-channel MOS transistor having a source and a drain formed of the N-type diffused layer 113 is formed.

[0005]

In the prior art standard cell, all the cells have the same constant width (height in Fig. 18(b)), and the VDD power supply line 120 and the VSS power supply line 121 having the same fixed width are located at an upper end portion and at a lower end portion of the cell, respectively, as shown in Fig. 18(b). An area between the pair of power supply lines in the cell is used to form the transistors included in the cell and to locate interconnections between terminals (contacts) within the cell ("in-cell wiring"). On the other hand, the routing channel has to be used for the interconnection between cells. However, the width of the cell is determined to meet a function cell such as a flipflop which needs a number of transistors and a complicated in-cell wiring. Therefore, a problem has

been encountered that, in a relatively simple function cell such as an inverter and a 2-input NAND gate which has a simple in-cell wiring, although there arise many empty areas for the first level metal, the empty areas could not be utilized for the inter-cell connection. Furthermore, another problem has been encountered that, the power supply lines extending through all the standard cells have the constant width, and it is not so easy to change the width of the power supply lines in accordance with the magnitude of a required power supply current.

[0006]

Under this situation, Japanese Patent Application Pre-examination Publication No. JP-A-06-169016 discloses a standard cell having an empty area which is provided between a power supply line and an in-cell wiring area and which can be utilized for the inter-cell connection. Fig. 19(a), shows a wiring area diagram of a standard cell in accordance with this second prior art. An empty area is provided between the VDD line 120 of the first level metal and an in-cell wiring area 122, and another empty area is provided between the VSS line 121 of the first level metal and the in-cell wiring area 122. These empty areas can be utilized for the inter-cell connection so as to realize an elevated integration density.

[0007]

In addition, Japanese Patent Application Pre-examination Publication No. JP-A-03-062551 discloses a standard cell having a device formation area extending into an outside of the power supply line. Fig. 19(b) shows a wiring area diagram of a standard cell in accordance with this third prior art. An in-cell wiring area 122 is provided between the VDD line 120 and the VSS line 121, similarly to the first prior art example shown in Fig. 18(b). However, a device formation area 125 depicted by a chain line extends into an outside of each power supply line. Since this outside area

can be utilized as a routing channel, the outside area can be utilized for the inter-cell connection. In addition, even if the position of the power supply lines is standardized for all the cells, it is possible to freely set a substantial cell width determined by the size of the device formation area.

[0008]

Furthermore, Japanese Patent Application Pre-examination Publication No. JP-A-05-055381 proposes a standard cell having no power supply line pattern. Fig. 19(c) shows a wiring area diagram of a standard cell in accordance with this fourth prior art. The standard cell includes only an in-cell wiring area 122 including transistors formed in the cell and a wiring pattern for connecting between terminals in the cell. After the standard cells are placed in the form of an array, a power supply line pattern which has a line width determined on the basis of the length of the cell array and a power consumption, is generated to connect to each standard cells. Therefore, the power supply line can have an optimum line width.

[0009]

[Problem that the invention is intended to solve]

However, the standard cell of the second prior art are difficult to optimize the width of the power supply line, and are restricted to have a constant cell width. The standard cell of the third prior art is difficult to optimize the width of the power supply line. The standard cell of the fourth prior art are restricted to have a constant cell width. In addition, since the device formation area is not used for the inter-cell connection, the wiring density is low.

[0010]

Accordingly, it is an object of the present invention to provide a standard cell, a standard cell array, and a placing and routing system and a

placing and routing method of standard cells, capable of forming an inter-cell connection in an area between a power supply line and an in-cell wiring area and also capable of ensuring the power supply line having an optimum line width, without a restriction requiring a constant cell width.

[0011]

[Means for solving the problem]

A standard cell in accordance with a first aspect of the present invention is characterized in that it comprises a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of the first level metal. Furthermore, the standard cell in accordance with the present invention comprises a function circuit including at least one P-channel transistor and at least one N-channel transistor; a first power supply terminal for supplying a first power supply voltage to the at least one P-channel transistor, a second power supply terminal for supplying a second power supply voltage to the at least one N-channel transistor, and an input terminal and an output terminal for the function circuit, and is characterized in that the first power supply terminal is provided at a P-type diffused layer of the at least one P-channel transistor supplied with the first power supply voltage, and the second power supply terminal is provided at an N-type diffused layer of the at least one N-channel transistor supplied with the second power supply voltage and in that the input terminal and the output terminal for the function circuit are constituted of a first level metal.

[0012]

A standard cell array in accordance with a second aspect of the present invention, is characterized in that a plurality of standard cells in accordance with the first aspect of the present invention, are located in such a manner that respective well boundary lines within said standard cells are

aligned on one straight line, and a substrate contact cell for connecting a first power supply voltage and a second power supply voltage to said semiconductor substrate and a well formed in said semiconductor substrate, respectively, is inserted into said standard cell array at predetermined intervals, at least one for a predetermined number of standard cells.

[0013]

A standard cell placement and routing processing system in accordance with a third aspect of the present invention, is characterized in that it comprises a library file which stores information of various standard cells in accordance with a first aspect of the present invention, , a circuit connection information file which stores circuit connection information of an LSI to be developed, a constraint information file which stores constraint information concerning the placement and the routing, a parameter file which stores parameter information including a power supply voltage and an operating frequency of said LSI to be developed and a sheet resistance of said diffused layer, a placement and routing system for executing the placement and the routing of said standard cells by utilizing information from said library file, said circuit connection information file and said parameter file, and an input/output and display apparatus for displaying a history and a result of the placement and the routing and for externally inputting a control command to control said placement and routing system.

[0014]

A standard cell placement and routing method in accordance with a fourth aspect of the present invention, executed by using the standard cell placement and routing processing system in accordance with the third aspect of the present invention, is characterized in that the method comprises:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and locating the read-out standard cells into a plurality of standard cell arrays, each of said plurality of standard cell arrays including at least one substrate contact cell inserted for every a predetermined number of standards cells, and said standard cells included in each of said plurality of standard cell arrays being arranged in such a manner that respective well boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a third step of routing signal lines between the standard cells included in said standard cell array, in accordance with said circuit connection information;

a fourth step of extracting a contour of a wiring area of said signal lines within said standard cell array, and placing a power supply line at the outside of said wiring area;

a fifth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said diffused layer within said standard cell in said standard cell array, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then, forming a contact hole at an overlapping portion between said power supply line and said extended power supply line of said diffused layer;

a sixth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a seventh step of re-routing said signal lines between said standard cells when it is discriminated in said sixth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fourth step; and

an eighth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays when it is discriminated in said sixth step that the resistance of said power supply line of said diffused layer is not greater than said predetermined resistance value.

Here, said second step can include:

a first sub-step of reading out from said cell library file, said standard cells corresponding to the read-out circuit connection information, and locating said read-out standard cells into a plurality of standard cell arrays in such a manner that respective well boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a second sub-step of inserting said at least one substrate contact cell for every a predetermined number of standards cells in each standard cell array, to complete said plurality of standard cell arrays;

a third sub-step of calculating a power supply line width on the basis of information including the number of the standard cells and the kinds of the standard cells included said standard cell array, said power supply voltage, and said operating frequency;

a fourth sub-step of calculating the width of a routing channel required from said power supply line width, the number of signal lines, and signal paths; and

a fifth sub-step of discriminating whether or not the routing is possible, with reference to a chip size stored in said constraint information

file, and returning to said first sub-step when the routing is not possible, and on the other hand, completing said second step when the routing is possible.

Furthermore, said fifth step can include:

a first sub-step of extracting said power supply terminals of said standard cells included in said standard cell array;

a second sub-step of discriminating whether or not the extracted power supply terminal overlaps said power supply line;

a third sub-step of extending said power supply line of said diffused layer from said extracted power supply terminal to said power supply line when said extracted power supply terminal does not overlap said power supply line, so that said extended power supply line of said diffused layer overlaps said power supply line; and

a fourth sub-step of forming a contact hole at an overlapping portion between said extracted power supply terminal and said power supply line when it is discriminated in said second sub-step that said extracted power supply terminal overlaps said power supply line, or alternatively at an overlapping portion between said power supply line and said extended power supply line of said diffused layer when it is discriminated in said second sub-step that said extracted power supply terminal does not overlap said power supply line.

Moreover, said seventh step can include:

a first sub-step of detecting a signal line which becomes a hindrance in reducing the resistance of said power supply line formed of said diffused layer to not greater than said predetermined resistance value;

a second sub-step of removing said signal line which becomes said hindrance, and providing a through-hole for connecting between said first

level metal and a second level metal at an end position to which the removed signal line was connected; and

a third sub-step of discriminating whether or not the resistance of said power supply line formed of said diffused layer shortened as the result of the removal of said signal line is not greater than said predetermined resistance value, and returning to said first sub-step when the resistance is greater than said predetermined resistance value, or alternatively completing said seventh step when the resistance is not greater than said predetermined resistance value.

[0015] A standard cell placement and routing method in accordance with a fifth aspect of the present invention, executed by using the standard cell placement and routing processing system in accordance with the third aspect of the present invention, is characterized in that the method comprises:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and provisionally locating the read-out standard cells into a plurality of provisional standard cell arrays;

a third step of dividing said provisional standard cell array into a plurality of cell groups each including not greater than a predetermined number of standard cells which are located adjacent to one another;

a fourth step of selecting one cell group to be processed, from said plurality of cell groups;

a fifth step of routing signal lines between said standard cells within said one selected cell group;

a sixth step of extracting a contour of a wiring area of said signal lines within said one selected cell group, to register a power supply line inhibit area in said constraint information file;

a seventh step of placing a power supply line along the outside of said power supply line inhibit area within said one selected cell group;

an eighth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said diffused layer within said standard cell in said one selected cell group, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then, forming a contact hole at an overlapping portion between said power supply line and said power supply line of said diffused layer;

a ninth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a tenth step of re-routing said signal lines between said standard cells when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fifth step;

an eleventh step of discriminating whether or not the processing for all the cell groups has been completed, when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is not greater than said predetermined resistance value, and then, returning to said fourth step when the processing for all the cell groups has not yet been completed;

a twelfth step of replacing said provisional standard cell array composed of the provisionally located standard cells, with corresponding

cell groups processed above, when it is discriminated in said eleventh step that the processing for all the cell groups has been completed;

a thirteenth step of interconnecting respective power supply lines of said cell groups processed above to form a power supply line for said standard cell array; and

a fourteenth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays.

[0016]

[Embodiments]

Figs. 1(a) and 1(b) are pattern diagrams of one embodiment of the standard cell in accordance with the present invention. Fig. 1(a) illustrates patterns of all levels within an inverter cell 101. The reference number 111 designates an N-well, and the reference number 112 indicates a P-type diffused layer. The reference number 113 shows an N-type diffused layer, and the reference number 114 denotes a polysilicon. The reference number 115 designates a contact hole between the P-type or N-type diffused layer and a first level metal. The reference number 116 indicates a contact hole between the polysilicon and the first level metal. The reference number 117 shows the first level metal. The reference number 118 denotes a VDD terminal on the P-type diffused layer. The reference number 119 designates a VSS terminal on the N-type diffused layer. In the N-well 111, a P-channel MOS transistor having a source and a drain formed of the P-type diffused layer is formed, and the VDD terminal 118 is formed on the P-type diffused layer 112 which constitutes the source of the P-channel MOS transistor. Similarly, in a P-type substrate region at the outside of the N-well, an N-channel MOS transistor having a source and a drain formed of the N-type diffused layer 113 is formed, and the VSS terminal 119 is formed on the N-type diffused layer

which constitutes the source of the N-channel MOS transistor. Both of the transistors are connected by the first level metal 117 and the contact hole 115, so as to constitute an inverter.

[0017]

The pattern diagram of Fig. 1(b) illustrates only the P-type diffused layer, the N-type diffused layer and the first level metal shown in Fig. 1(a). Fig. 1(b) shows the VDD terminal 118 of the diffused layer, the VSS terminal 119 of the diffused layer, an input terminal IN of the first level metal, and an output terminal OUT of the first level metal. The standard cell in accordance with the present invention is characterized by having the VDD terminal 118 and the VSS terminal 119 of the diffused layer, and the input terminal IN and the output terminal OUT of the first level metal, without having a metal connection line for a power supply line.

[0018]

In the standard cell in accordance with the present invention, since the power supply terminal is constituted of the diffused layer, the standard cell is connected to a power supply metal line through a wiring conductor formed of the diffused layer, with the result that it is in some cases that a parasite resistance is inserted between the power supply metal line and the transistor. However, with a recent advanced metal silicide forming technology, a titanium silicide which is formed by depositing a metal titanium (Ti) on a surface of a diffused region and converting the metal titanium into titanium silicide, and a cobalt silicide which is formed by depositing a metal cobalt (Co) on a surface of a diffused region and converting the metal cobalt into cobalt silicide, have been reduced into practice, with the result that a sheet resistance of the diffused layer has been drastically reduced. Therefore, it is possible to minimize the parasitic resistance to a value generating no practical hindrance.

[0019]

Fig. 2(a) is a pattern diagram of a 2-input NOR cell 102, and Fig. 2(b) is a pattern diagram of a 2-input NAND cell 103. Fig. 3(a) is a pattern diagram of a low power inverter cell 104, and Fig. 3(b) is a pattern diagram of a substrate contact cell 105 for fixing the potential of the N-well 111 and the potential of the P-type substrate to the VDD potential and the VSS potential, respectively. As shown in Figs. 1(a), 1(b), 2(a), 2(b), 3(a) and 3(b), the standard cells in accordance with the present invention can have not only different cell lengths but also different cell widths.

[0020]

Fig. 4 is a constructional diagram of a standard cell placement and routing processing system for performing the placement and routing by using the standard cells in accordance with the present invention so as to design an LSI. The design system comprises a placement and routing system 401 for performing the placement of cells and the routing of the inter-cell connections and the power supply lines, a cell library file 402 including the standard cells shown in Figs. 1(a), 1(b), 2(a), 2(b), 3(a) and 3(b), a circuit connection information file 403 for a circuit connection information of the LSI to be developed, a constraint information file 404 storing various constraints concerning the placement and routing, an input/output and display apparatus 405, and a parameter file 406 storing various information including an operating frequency, an operating temperature range, a sheet resistance of a P-type diffused layer, an N-type diffused layer and various interconnection metal layers. The input/output and display apparatus 405 can display the history and the result of the placement and routing, and various commands can be inputted through the input/output and display apparatus 405 to control the execution of the placement and routing.

[0021]

Now, the placement and routing method executed in the placement and routing system 401 will be described in detail. Fig. 5 is a flow chart of the placement and routing method.

[0022]

In a step 501, a circuit connection information which represents a circuit of the LSI by small circuits corresponding to cell functions and connection information between the small circuits, is picked up from the circuit connection information file 403, and the processing goes into a step 502.

[0023]

Fig. 6 is a circuit diagram of a circuit example represented by the circuit connection information inputted in the step 501. An input terminal of a low power inverter 604 is connected to a terminal A, and an output terminal of the low power inverter 604 is connected through a connection line A1 to one input terminal of a 2-input NAND circuit 603. The other input terminal of the 2-input NAND circuit 603 is connected to a terminal B, and an output terminal of the 2-input NAND circuit 603 is connected through a connection line A2 to one input terminal of a 2-input NOR circuit 602. The other input terminal of the 2-input NOR circuit 602 is connected to a terminal C, and an output terminal of the 2-input NOR circuit 602 is connected through a connection line A3 to an input terminal of an inverter 601. An output terminal of the inverter is connected to a terminal D. Here, the inverter 601, the 2-input NOR circuit 602, the 2-input NAND circuit 603 and the low power inverter 604 are one small circuit, respectively, and correspond to the inverter cell 101, the 2-input NOR cell 102, the 2-input NAND cell 103 and the low power inverter cell 104, respectively.

[0024]

In a step 502, standard cells corresponding to the circuit connection information is read out from the cell library file 402, and the read-out standard cells are assorted for each cell array. In each cell array, the standard cells are placed in such a manner that a boundary line of the N-well 111 in the respective standard cells are aligned on one straight line in a plan view.

Fig. 7 is a flow chart showing the details of the processing in the step 502. In a step 701, a provisional placement order of the small circuits included in the circuit connection information is determined on the basis of the number of interconnection lines between the small circuits and a proximity placement constraint from the constraint information file 404. Then, the standard cells corresponding to the small circuits are read out from the cell library file 402, and the small circuits are replaced by the read-out standard cells, respectively. Furthermore, the length of the cell array and the number of cells included in the cell array are adjusted, and the positions of the read-out standard cells are determined in such a manner that a boundary line of the N-well 111 in the respective standard cells are aligned on one straight line in a plan view. Thus, a provisional cell array is completed.

In a next step 702, in order to stably fix the potential of the N-well in each standard cell to the VDD potential and also to stably fix the potential of the P-type substrate to the VSS potential, at least one substrate contact cell 105 is inserted for every a predetermined number of cells in the provisional cell array, so that a standard cell array is formed.

Succeedingly, in a step 703, an optimum power supply line width for each standard cell array is calculated by considering a heat generation caused by an electric power consumption and an electromigration

resistance, which are obtained on the basis of the number of cells and the kinds of cells included in the standard cell array, as well as various information read out from the parameter file 406, including the sheet resistance of the first level metal, the power supply voltage, the operating frequency, and the operating temperature.

Then, in a step 704, a routing channel required between each pair of adjacent standard cell arrays is calculated from the optimum power supply line obtained in the preceding step 703, the number of signal lines between cells, rough signal paths, and the width of wiring enabling areas within the standard cell array.

Thereafter, in a step 705, the chip size of the LSI is estimated from the standard cell arrays and the routing channels thus obtained, and whether or not the chip size of the LSI thus estimated meets a vertical size and a horizontal size of the chip stored in the constraint information file 404, is discriminated. If the estimated chip size does not meet the vertical size and the horizontal size of the chip, the processing returns to the step 701 so that a command is inputted through the input/output and display apparatus 405 to increase or decrease the number of cell arrays for relocation. If the estimated chip size meets the vertical size and the horizontal size of the chip, the step 502 is completed, and the processing goes to a step 503.

[0025]

Fig. 8 is a pattern diagram of a portion of the standard cell array when the processing of the step 502 is completed. The inverter cell 101, the 2-input NOR cell 102, the 2-input NAND cell 103 and the low power inverter cell 104, which correspond to the inverter 601, the 2-input NOR circuit 602, the 2-input NAND circuit 603 and the low power inverter 604 shown in Fig. 6, respectively, are closely placed in such a manner that the boundary line of the N-well 111 in the respective standard cells are aligned

on one straight line in a plan view, and further, the substrate contact cell 105 is added. The respective N-wells 111 of the standard cells are coupled to form one continuous pattern. In addition, since the respective standard cells have different widths, respectively, the standard cell array shown in Fig. 8 has an upper boundary or contour line and a lower boundary or contour line, both of which are bumpy or unstraight.

[0026]

In a step 503, the routing of signal lines in each standard cell array is carried out in accordance with the circuit connection information stored in the circuit connection information file 403. Fig. 9 is a pattern diagram of the same portion of the standard cell array when the processing of the step 503 is completed. In accordance with the circuit connection shown in Fig. 6, the terminal A is connected to the input terminal of the low power inverter cell 104 through an interconnection line 901 of the first level metal. The output terminal of the low power inverter cell 104 is connected to one input terminal of the 2-input NAND cell 103 through an interconnection line 901 (A1) of the first level metal. The terminal B is connected to the other input terminal of the 2-input NAND cell 103 through an interconnection line 901 of the first level metal. The output terminal of the 2-input NAND cell 103 is connected to one input terminal of the 2-input NOR cell 102 through an interconnection line 901 (A2) of the first level metal. The output terminal of the 2-input NOR cell 102 is connected to the input terminal of the inverter cell 101 through an interconnection line 901 (A3) of the first level metal. The output terminal of the inverter cell 101 is connected to the terminal D through an interconnection line 901 of the first level metal. Thus, if the step 503 is completed, the processing goes to a step 504.

[0027]

In the step 504, a contour of wiring areas within the standard cell array is extracted, and a power supply line is located at the outside of the contour. Referring to Fig. 11, a VDD power supply line 1101 is located at an upper outside of the metal signal lines of the first level metal within the cell array in the plan view, and a VSS power supply line 1102 is located at a lower outside of the metal signal lines of the first level metal within the cell array in the plan view.

[0028]

Then, the processing goes to the step 505, in which the power terminals of each cell are connected to the power supply lines. Fig. 10 is a flow chart of the details of the processing in the step 505. In a step 1001, one standard cell VDD terminal 118 included in the standard cell array is extracted. In a step 1002, whether or not the extracted VDD terminal 118 overlaps the VDD power supply line 1101, is discriminated. If the extracted VDD terminal 118 overlaps the VDD power supply line 1101, the processing goes to a step 1004. On the other hand, if the extracted VDD terminal 118 does not overlap the VDD power supply line 1101, the processing goes to a step 1003, in which a power supply line formed of a P-type diffused layer 1103 (Fig. 11) for supplying the VDD voltage is extended from the VDD terminal 118 towards the VDD power supply line 1101, and also the N-well pattern is correspondingly extended to surround the power supply line formed of a P-type diffused layer 1103, so that the power supply line formed of the P-type diffused layer 1103 extending from the VDD terminal 118 overlaps the VDD power supply line 1101. After the step 1003 is completed, the processing goes to the step 1004.

In the step 1004, a contact pattern 1105 for interconnecting between the diffused layer and the first level metal is generated and located at an overlapping portion between the VDD power supply line 1101 and the

VDD terminal 118 or at an overlapping portion between the VDD power supply line 1101 and the extended power supply line formed of the P-type diffused layer 1103.

In a next step 1005, whether or not a processing for connecting all the VDD terminals 118 to the VDD power supply line 1101 has been completed, is discriminated. If the connecting processing for all the VDD terminals 118 has not yet been completed, the processing returns to the step 1001. On the other hand, if the connecting processing for all the VDD terminals 118 has been completed, the processing for the VDD terminals 118 is ended, Then, a processing for connecting the VSS terminals 119 to the VSS power supply line will be performed. This connecting processing for the VSS terminals 119 is similar to the above mentioned connecting processing for the VDD terminals 118, and therefore, can be easily understood from the above description from the steps 1001 to 1005 by replacing the VDD terminal 118, the VDD power supply line 1101 and the power supply line formed of the P-type diffused layer, with the VSS terminal 119, the VSS power supply line 1102 and a power supply line formed of an N-type diffused layer, respectively. If the connecting processing for all the VDD terminals 118 and the VSS terminals 119 has been completed, the processing goes to a step 506.

[0029]

Fig. 11 is the pattern diagram of the same portion of the standard cell array when the processing of the step 505 is completed. The VDD power supply line 1101 and the VSS power supply line 1102 are located at the outside of an area in which the in-cell wiring lines and the inter-cell connections are located. The contact hole 1105 is formed at the overlapping portion between the VDD terminal 118 and the VDD power supply line 1101. In the VDD terminal 118 that does not overlap the

VDD power supply line 1101, the power supply line formed of the P-type diffused layer 1103 is formed to extend from the VDD terminal 118 to the VDD power supply line 1101, and the contact hole 1105 is formed at the overlapping portion between the VDD power supply line 1101 and the extended power supply line formed of the P-type diffused layer 1103 for the purpose for connecting the VDD power supply line 1101 to the VDD terminal 118 that does not overlap the VDD power supply line 1101. Similarly, in the VSS terminal 119 that does not overlap the VSS power supply line 1102, the power supply line formed of the N-type diffused layer 1104 is formed to extend from the VSS terminal 119 to the VSS power supply line 1102, and the contact hole 1105 is formed at the overlapping portion between the VSS power supply line 1102 and the extended power supply line formed of the N-type diffused layer 1104 for the purpose for connecting the VSS power supply line 1102 to the VSS terminal 119 that does not overlap the VSS power supply line 1102.

[0030]

In the step 506, whether or not the resistance of the power supply line formed of the P-type diffused layer 1103 and the power supply line formed of the N-type diffused layer 1104 is in a permitted limit, is ascertained. For this purpose, the respective sheet resistance of the P-type diffused layer and the N-type diffused layer are read out from the parameter file 406, and the resistance value is calculated from the width and the length of the diffused layer constituting the power supply line, and is compared with a permissible resistance value stored in the constrain information film 404. If the resistance of all the power supply lines formed of the diffused layer is not greater than the permissible resistance value, the processing goes to a step 508. If the resistance of at least one

power supply line formed of the diffused layer is greater than the permissible resistance value, the processing goes to a step 507.

[0031]

In the step 507, a re-routing is carried out for making the resistance of all the power supply lines formed of the diffused layer not greater than the permissible resistance value. Fig. 12 is a flow chart of the details of the re-routing processing in the step 507. In a step 1201, the signal line formed of the first level metal which becomes a bottle neck in reducing the resistance of the (first-aimed) power supply line formed of the diffused layer to not greater than the permissible resistance value, is detected. In a succeeding step 1202, the detected signal line formed of the first level metal becoming the bottle neck is removed, and a through-hole for connecting to a second level metal is located at a position to which each end of the removed signal line was connected. At the same time, the corresponding power supply line of the first level metal and the power supply line formed of the diffused layer having the resistance which is greater than the permissible resistance value and which therefore is to be reduced by removing the signal line formed of the first level metal, are removed. The processing goes into a step 1203. In the step 1203, the size of the power supply line formed of the diffused layer which can be shortened as the result of the processing in the step 1202, is estimated, and the resistance value of the estimated power supply line is calculated and then compared with the permissible resistance value. If the resistance value is greater than the permissible resistance value, the processing returns to the step 1201. To the contrary, if the resistance value is not greater than the permissible resistance value, the re-routing for the (first-aimed) power supply line formed of the diffused layer in question, is completed, and a similar processing is repeated for other power supply lines formed of

the diffused layer having the resistance greater than the permissible resistance value. If the re-routing is completed for all the power supply lines formed of the diffused layer having the resistance greater than the permissible resistance value, since all the power supply lines formed of the diffused layer have a resistance not greater than the permissible resistance value, the processing goes to a step 508.

[0032]

In the step 508, interconnections that have not yet been connected within the cell array, are generated, and signal lines are connected between the standard cell arrays. Thus, the placement and routing processing is completed.

[0033]

Figs. 13(a), 13(b), 13(c) and 13(d) are layout diagrams illustrating the interconnection condition in the standard cell array at various steps in the placement and routing process. Fig. 13(a) shows a layout diagram when the step 503 shown in Fig. 5 is completed. The standard cell array comprises a plurality of function cells 100 having different widths and each including a plurality of power supply terminals formed of the diffused layer, and at least one input terminal and one output terminal formed of the first level metal, and at least one substrate contact cell 105 provided for every a predetermined number of function cells. These function cells and the at least one substrate contact cell are placed in the form of an array in such a manner that the boundary line of the N-well in the respective standard cells are aligned on one straight line in a plan view. In addition, interconnections 901 formed of the first level metal are placed for the inter-cell connection. Furthermore, an area of the in-cell wiring and the inter-cell connections within the standard cell array, is confined as an inhibit area 1301 for inhibiting placement of the power supply line.

Fig. 13(b) shows a layout diagram when the step 505 shown in Fig. 5 is completed. The VDD power supply line 1101 and the VSS power supply line 1102 are located at the outside of the inhibit area 1301, and the power supply line 1103a formed of the P-type diffused layer is provided. Here, assume that the power supply line 1103a formed of the P-type diffused layer has a resistance greater than the permissible resistance value.

Fig. 13(c) shows a layout diagram when the step 1202 shown in Fig. 12 is completed in the course of the re-routing processing of the step 507. The power supply line 1103a formed of the P-type diffused layer and the VDD power supply line 1101 are removed, and the interconnections 901a and 901b of the first level metal which become a bottle neck in reducing the resistance of the power supply line 1103a formed of the P-type diffused layer, are removed. Furthermore, through-holes 1302 are located at end positions of the interconnections 901a and 901b.

Fig. 13(d) shows a layout diagram when the step 508 is completed. The VDD power supply line 1101 is re-placed at the outside of a modified inhibit area 1301a, and in place of the removed interconnections 901a and 901b of the first level metal, interconnections 1303 of a second level metal, the through-holes 1302 and the interconnections 901 of the first level metal are formed so that the interconnections detour to pass at the outside of the VDD power supply line 1101. As a result, a new power supply line 1103b formed of the P-type diffused layer can have a reduced length and therefore a reduced resistance which is in the permissible resistance limit.

[0034]

The inter-array connection is also executed in the step 508. Fig. 14 is a pattern diagram when the processing of the step 508 is completed. An inter-array connection is formed by an interconnection line 901 of the first level metal extending from the terminal C, a through-hole 1302 formed

between the first level metal and the second level metal, an interconnection line 1303 of the second level metal, a through hole 1302 formed between the first level metal and the second level metal, so that the terminal C is connected to the other input of the 2-input NOR cell 102.

[0035]

As mentioned above, by forming the standard cell array by using the standard cells in accordance with the present invention, and routing the signal lines and the power supply lines in accordance with the flow chart of Fig. 5, it is possible to place and route standard cells having different widths with no hindrance, and it is also possible to set the width of the power supply line (of metal) to an appropriate width for each standard cell array. In addition, the device formation region can be utilized as a routing channel. Therefore, a high wiring density can be realized.

Fig. 15 is a flow chart of another embodiment of the method in accordance with the present invention for placing and routing standard cells. This is different from the flow shown in Fig. 5 in that, before forming the cell array, cell groups each including a plurality of cells of not greater than a predetermined number are formed, and in each cell group, the inter-cell connection and the power supply lines are placed and routed, and thereafter, the cell groups are coupled to form a cell array, and inter-group connections are executed.

[0036]

In a step 1501, circuit connection information is inputted. Then, in a step 1502, cells are provisionally placed to form a provisional cell array. In a step 1503, the provisional cell array is divided into a plurality of cell groups each consisting of not greater than a predetermined number of cells located adjacent one another in the same provisional cell array. At this time, it is possible to modify the circuit connection information in

accordance with to the cell groups thus obtained, and to store the modified circuit connection information in the circuit connection information file 403.

[0037]

Thereafter, the processing goes into a step 1504, in which one cell group is extracted. Then, in a step 1505, the standard cells included in the extracted cell group are read out from the cell library 402, and placed on the basis of a provisional placement information. In addition, at least one substrate contact cell is added, and the inter-cell connection is executed.

[0038]

Next, the processing goes into a step 1506, in which a power supply line inhibit area surrounded by an imaginary line along the contour of an area of signal lines within the cell group is extracted, and then, stored in the constraint information file. In a step 1507, an optimum width of a power supply line is calculated on the basis of the information stored in the constraint information file 404 and the parameter file 406, to generate a power supply line at the outside of the inhibit area. The power supply line may extend in a straight line but may be bent to extend along the contour of the inhibit area.

[0039]

Thereafter, the processing goes into a step 1508, in which the power supply terminals of the standard cells included in the cell group are connected to the power supply lines. When the power supply terminal overlaps the power supply line, a contact hole is generated at an overlapping position between the power supply line and the power supply terminal. If the power supply terminal does not overlap the power supply line (formed of metal), a power supply line of a diffused layer is extended from the power supply terminal to overlap the power supply line (formed

of metal), and a contact hole is generated at an overlapping position between the power supply line (formed of metal) and the extended power supply line of the diffused layer.

[0040]

In a step 1509, whether or not the resistance value of the power supply line of the diffused layer extending from the power supply terminal is in a permissible limit, is discriminated. If the resistance is greater than a permissible value, the processing goes into a step 1510, in which a processing similar to the flow chart shown in Fig. 12 is executed for re-routing. If the step 1510 is completed, the processing returns to the step 1505. When the resistance of all the power supply lines of the diffused layer is in the permissible limit, it is considered that the placement and routing processing for the cell group concerned has been completed, and the processing goes into a step 1511.

[0041]

In the step 1511, whether or not the placement and routing processing for all the cell groups has been completed, is discriminated. If the placement and routing processing for all the cell groups has not yet been completed, the processing returns to the step 1504. On the other hand, if the placement and routing processing for all the cell groups has been completed, the processing goes into a step 1512.

[0042]

In the step 1512, the provisionally placed cells in the provisional cell array are replaced with the cell groups processed mentioned above. In a next step 1513, the power supply lines are connected between the cell groups. Thereafter, in a step 1514, interconnections that have not yet been connected within the cell array, are generated, and signal lines are

connected between the standard cell arrays. Thus, the placement and routing processing is completed.

[0043]

Figs. 16(a), 16(b) and 16(c) are layout diagrams of various cell groups. Each cell group includes a plurality of function cells 100, one substrate contact cell 105, an inhibit area 1301 confined to surround a wiring area of the signal lines within the cell group, and the VDD power supply line 1101 and the VSS power supply line 1102 placed to extend along the outside of the inhibit area 1301. Fig. 16(d) is a layout diagram of the standard cell array obtained by coupling the cell groups shown in Figs. 16(a), 16(b) and 16(c).

[0044]

Fig. 17 is a pattern diagram of one cell group when the processing of the step 1508 is completed. The power supply line inhibit area 1301 is confined to surround the internal wiring area. The VDD power supply line 1101 is placed in a bent form to extend along the upper outside of the inhibit area 1301 in a plan view, and similarly, the VSS power supply line 1102 is placed in a bent form to extend along the lower outside of the inhibit area 1301 in a plan view. Because of the bent power supply lines, a further high wiring density can be realized, and also, the power supply line formed of the diffused layer for connecting between the power supply terminal and the power supply line (formed of metal) can be shortened in comparison with the pattern diagram shown in Fig. 11. Therefore, the number of the power supply lines formed of the diffused layer having the resistance greater than the permissible value, which are detected in the step 1509, can be reduced, with the result that efficiency of the placement and routing can be elevated.

[0045]

[Advantage of Invention]

As mentioned above, by forming the standard cell array by using the standard cells in accordance with the present invention, and routing the signal lines and the power supply lines in accordance with the present invention, it is possible to place and route standard cells having different widths with no hindrance, and it is also possible to utilize the device formation region between the power supply line and the wiring area within the cell, as a routing channel, with the result that a high wiring density can be realized. In addition, it is possible to set the width of the power supply line (of metal) to an appropriate width for each standard cell array.

[Brief Description of the Drawings]

[Fig. 1] is that Figs. 1(a) and 1(b) are pattern diagrams of an inverter cell which is one embodiment of the standard cell in accordance with the present invention.

[Fig. 2] is that Fig. 2(a) is a pattern diagram of a 2-input NOR cell which is one embodiment of the standard cell in accordance with the present invention, and Fig. 2(b) is a pattern diagram of a 2-input NAND cell which is one embodiment of the standard cell in accordance with the present invention.

[Fig. 3] is that Fig. 3(a) is a pattern diagram of a low power inverter cell which is one embodiment of the standard cell in accordance with the present invention, and Fig. 3(b) is a pattern diagram of a substrate contact cell which is one embodiment of the standard cell in accordance with the present invention.

[Fig. 4] is a constructional diagram of a processing system in accordance with the present invention for placing and routing standard cells.

[Fig. 5] is a flow chart of one embodiment of the method in accordance with the present invention for placing and routing standard cells.

[Fig. 6] is a circuit diagram of a circuit used for illustration.

[Fig. 7] is a flow chart of the details of the processing in the step 502 shown in Fig. 5.

[Fig. 8] is a pattern diagram when the processing of the step 502 is completed.

[Fig. 9] is a pattern diagram when the processing of the step 503 is completed.

[Fig. 10] is a flow chart of the details of the processing in the step 505 shown in Fig. 5.

[Fig. 11] is a pattern diagram when the processing of the step 505 is completed.

[Fig. 12] is a flow chart of the details of the processing in the step 507 shown in Fig. 5.

[Fig. 10] is that Figs. 13(a), 13(b), 13(c) and 13(d) are layout diagrams at various steps in the placement and routing process.

[Fig. 14] is a pattern diagram when the processing of the step 508 is completed.

[Fig. 15] is a flow chart of another embodiment of the method in accordance with the present invention for placing and routing standard cells.

[Fig. 16] is that Figs. 16(a), 16(b) and 16(c) are layout diagrams of various cell groups, and Fig. 16(d) is a layout diagram of the standard cell array.

[Fig. 17] is a pattern diagram when the processing of the step 1508 is completed.

[Fig. 18] is that Fig. 18(a) is a layout diagram of a standard cell type LSI, and Fig. 18(b) is a pattern diagram of a first prior art standard cell example.

[Fig. 19] is that Figs. 19(a), 19(b) and 19(c) are wiring area diagrams of second, third and fourth prior art standard cell examples.

[Explanation of Reference Characters]

100, 106, 106a function cell
101...inverter cell
102...2-input NOR cell
103 2-input NAND cell
104 low power inverter cell
105 substrate contact cell
111 N-well
112 P-type diffused layer
113 N-type diffused layer
114 polysilicon
115, 116, 1105 contact hole
117 first level metal
118 VDD terminal
119 VSS terminal
401...placement and routing system
402 cell library file
403 circuit connection information file
404 constraint information file
405 input/output and display apparatus
406 parameter file
901, 901a, 901b interconnection line of first level metal
1101 VDD power supply line

1102 VSS power supply line

1103, 1103a, 1103b power supply line of P-type diffused layer

1104 power supply line of N-type diffused layer

1301 inhibit area

1302 through-hole

1303 interconnections of second level metal

1801 routing channel

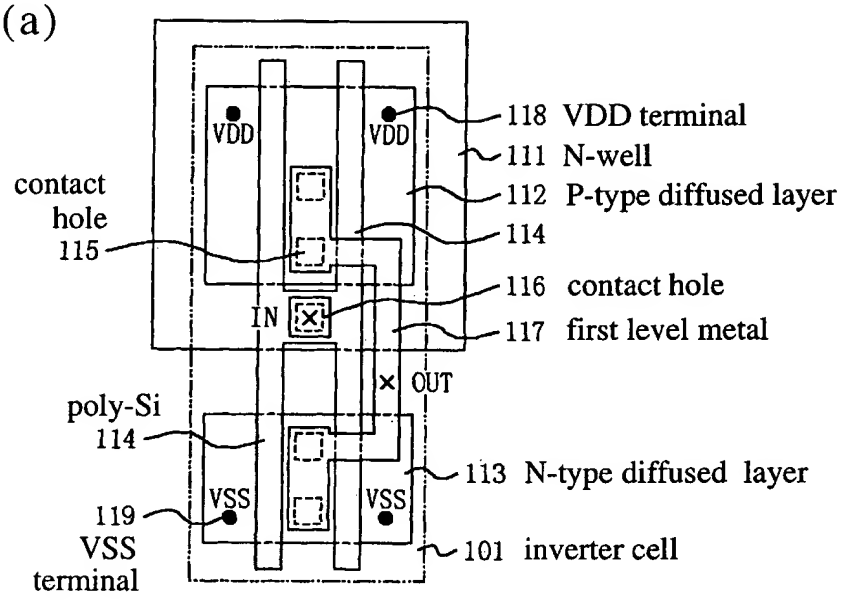
1802 inter-cell connection

1803 inter-array connection

[Name of Document] DRAWINGS

Fig. 1

(a)



(b)

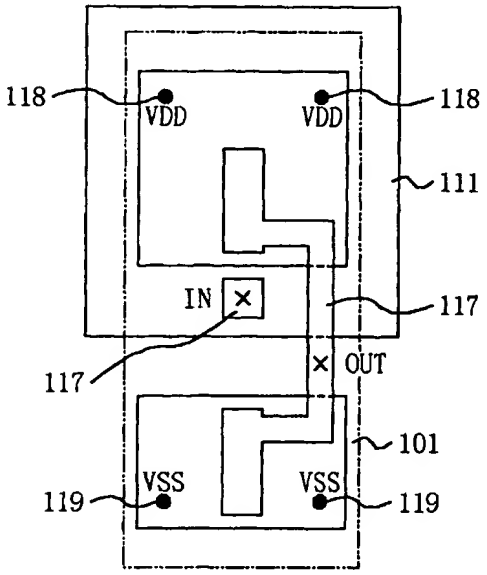
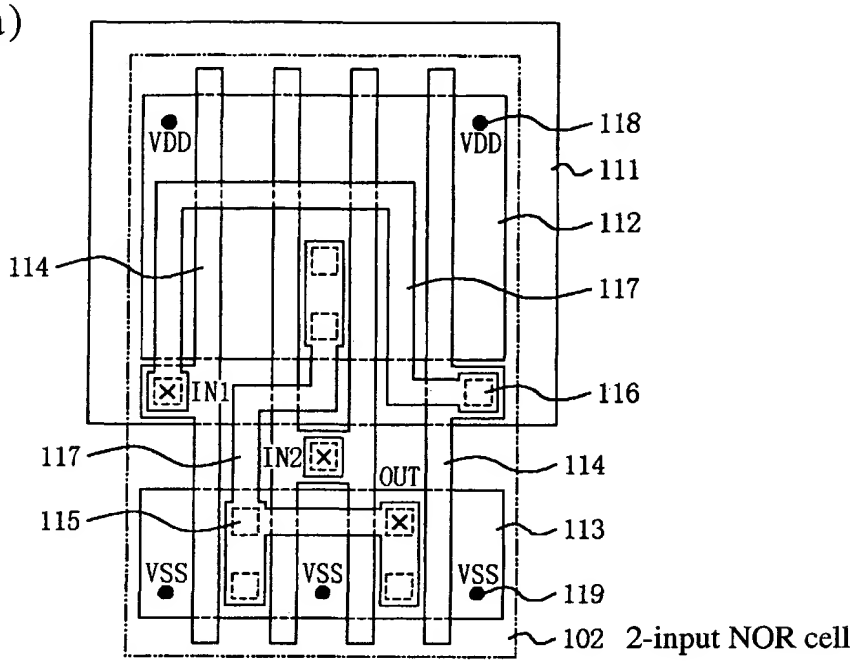


Fig. 2

(a)


VDD
VDD
118
111
112
114
117
IN1
116
117
IN2
OUT
114
115
113
VSS
VSS
VSS
119
102 2-input NOR cell

(b)

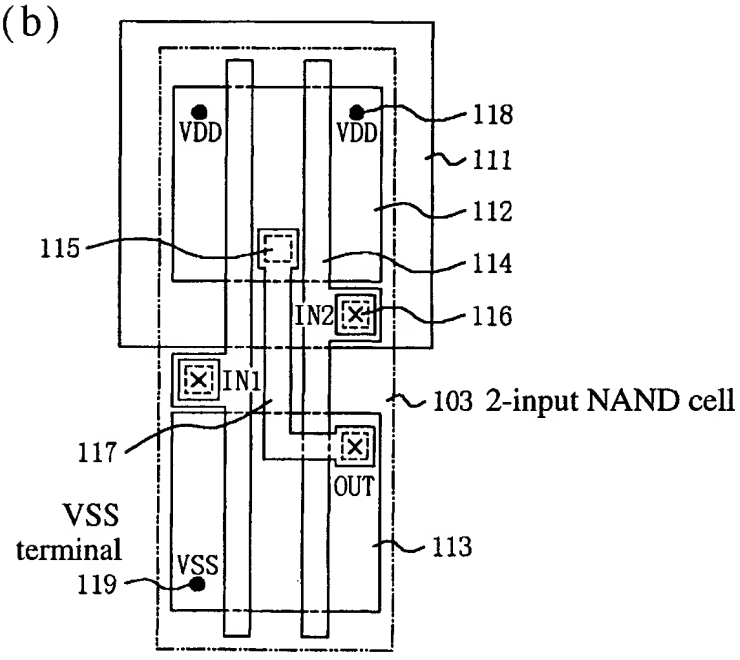
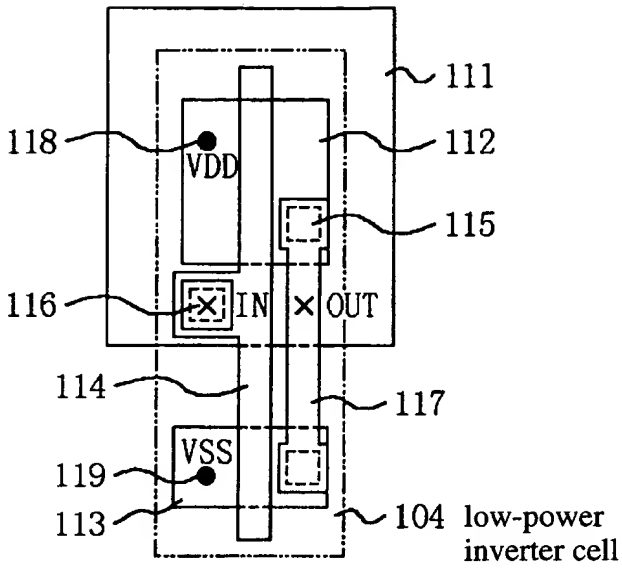

VDD
VDD
118
111
112
115
114
IN2
116
IN1
103 2-input NAND cell
117
OUT
VSS
terminal
113
VSS
119

Fig. 3

(a)


111
118
VDD
112
115
116
IN
OUT
114
117
VSS
119
113
104 low-power inverter cell

(b)

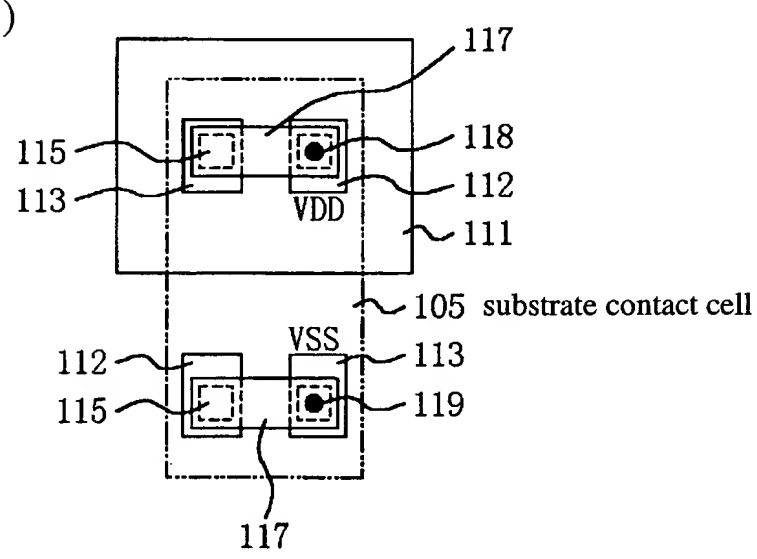

117
115
118
113
112
VDD
111
105 substrate contact cell
VSS
112
113
115
119
117

Fig. 4

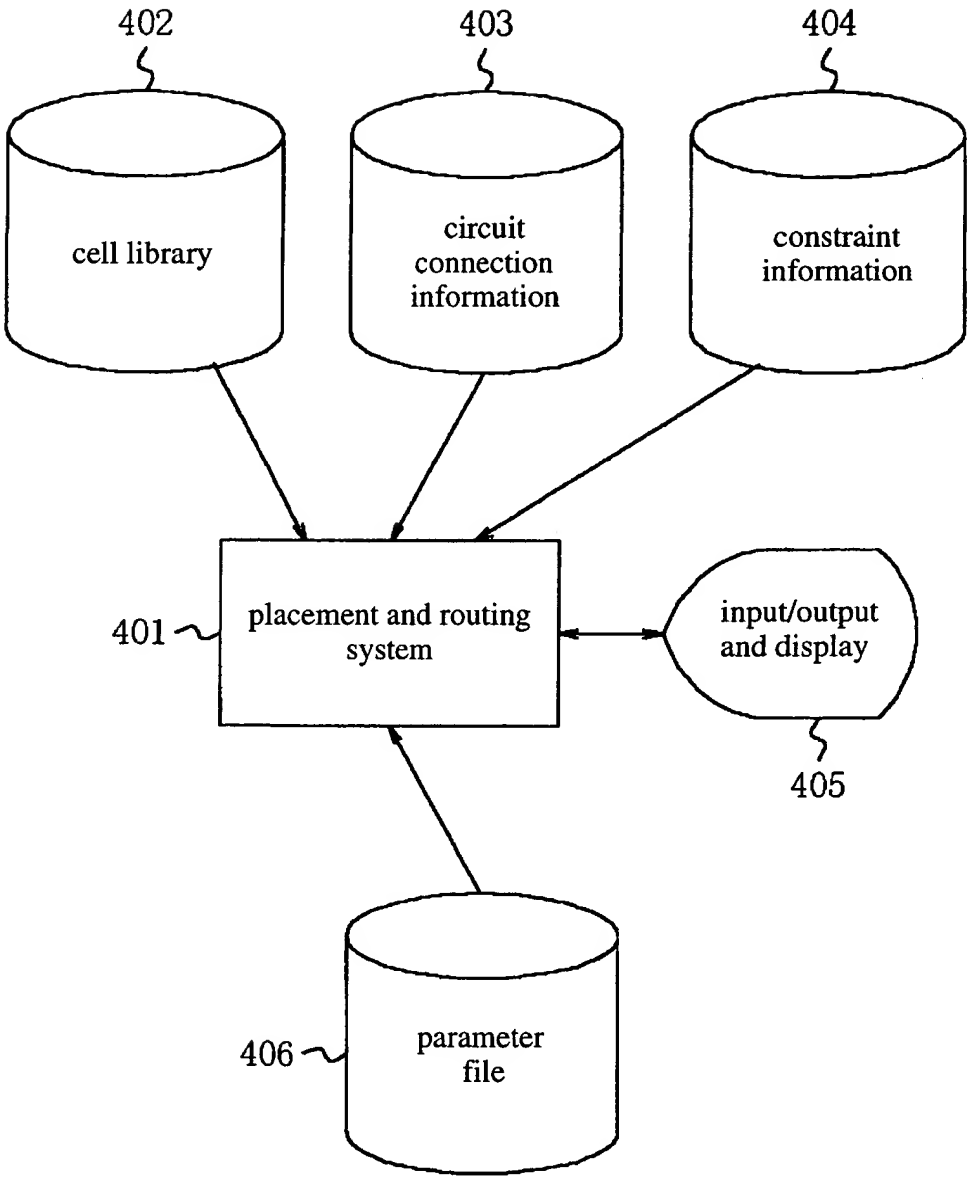

402
403
404
cell library
circuit connection information
constraint information
401
placement and routing system
input/output and display
405
406
parameter file

Fig. 5

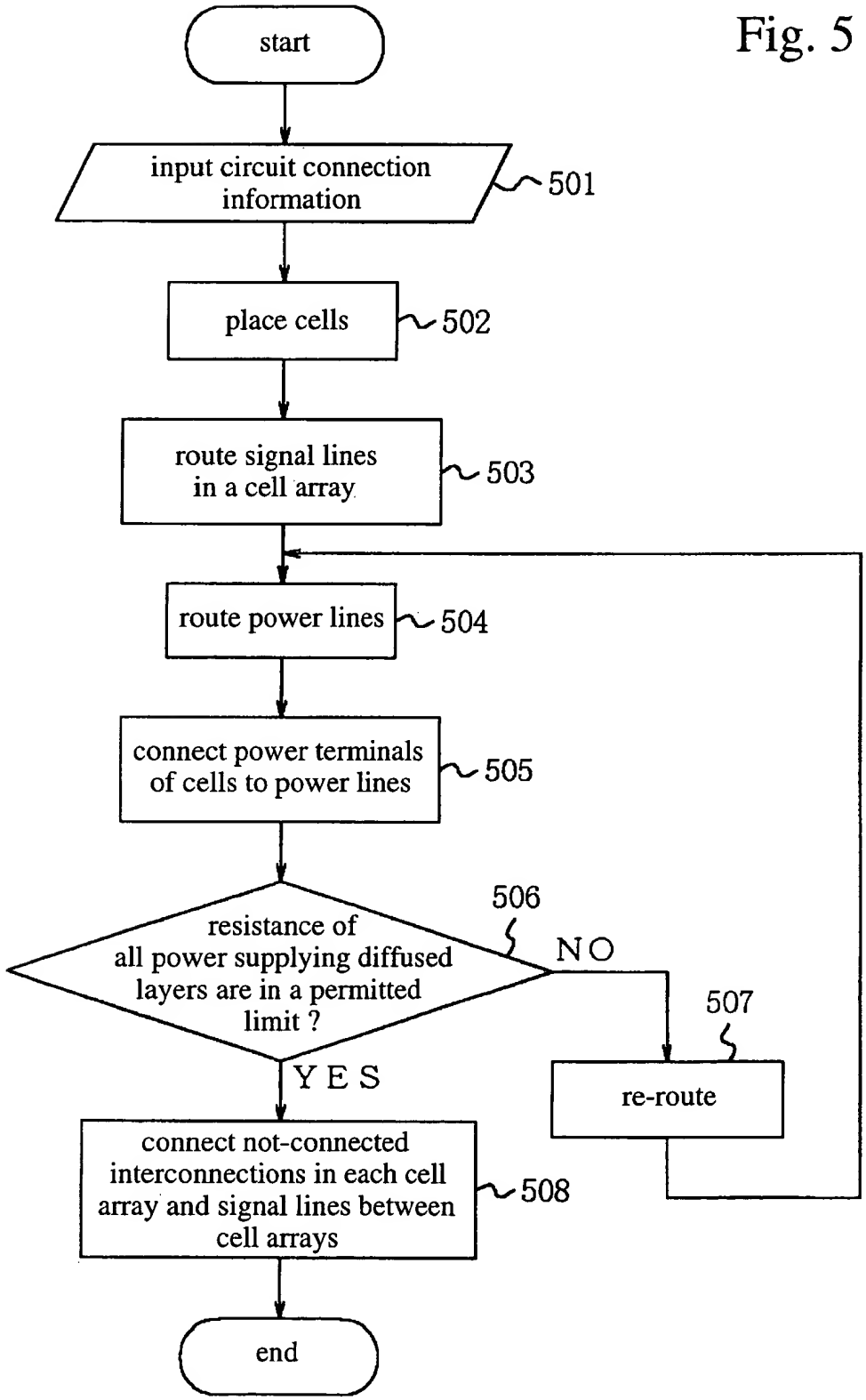

start
input circuit connection information
501
place cells
502
route signal lines in a cell array
503
route power lines
504
connect power terminals of cells to power lines
505
resistance of all power supplying diffused layers are in a permitted limit ?
506
NO
YES
507
re-route
connect not-connected interconnections in each cell array and signal lines between cell arrays
508
end

Fig. 6

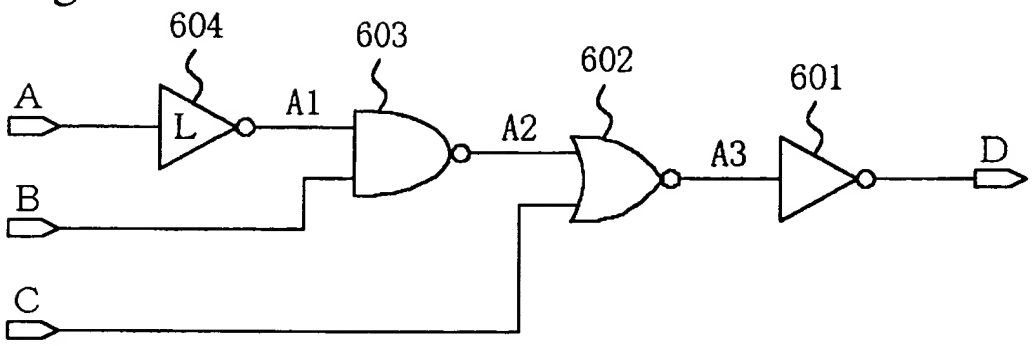


Fig. 7

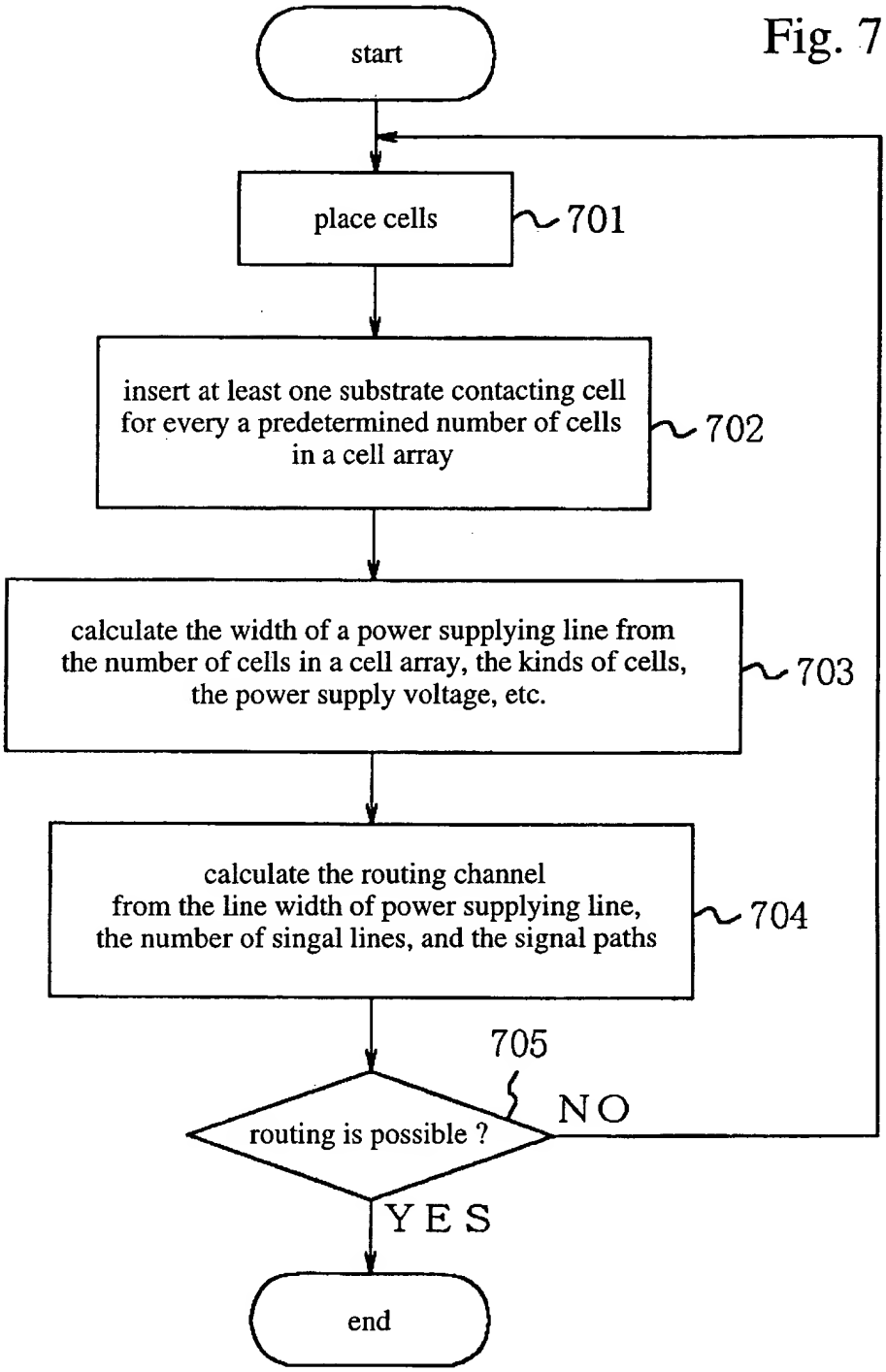

start
place cells
701
insert at least one substrate contacting cell for every a predetermined number of cells in a cell array
702
calculate the width of a power supplying line from the number of cells in a cell array, the kinds of cells, the power supply voltage, etc.
703
calculate the routing channel from the line width of power supplying line, the number of singal lines, and the signal paths
704
705
routing is possible ?
NO
YES
end

Fig. 8

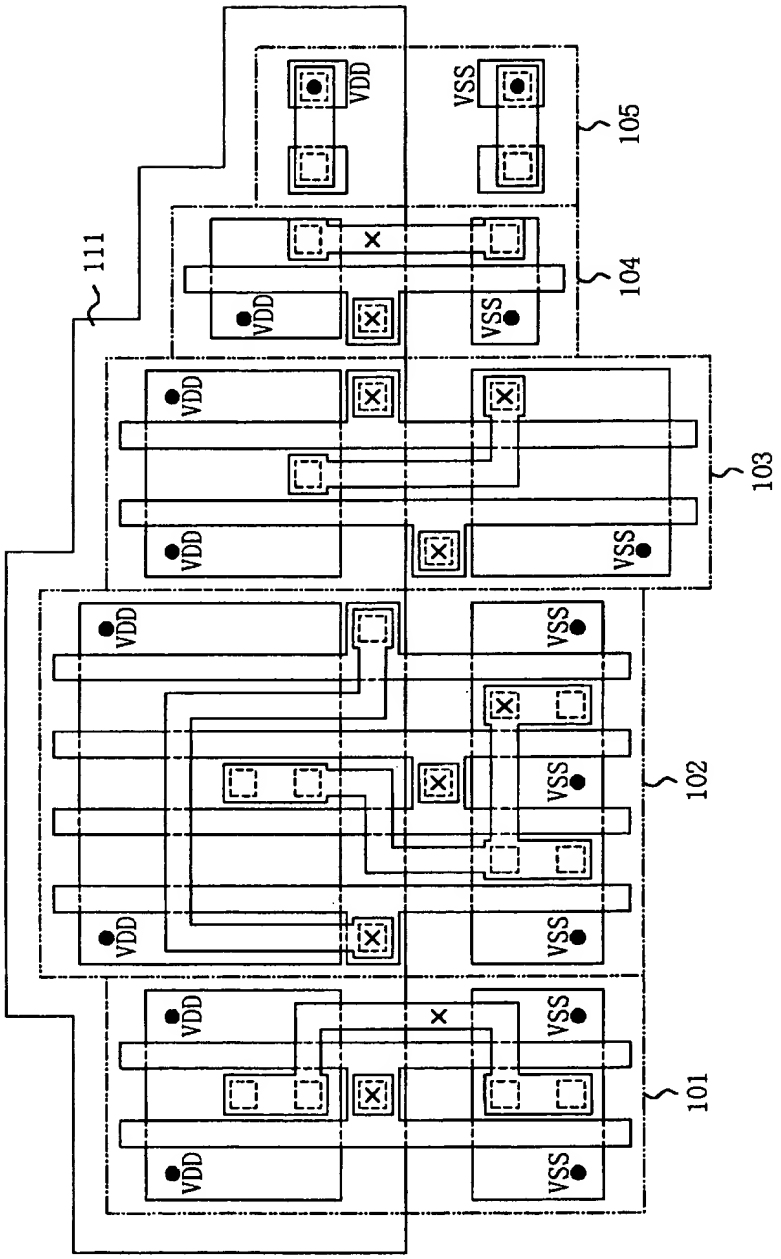


Fig. 9

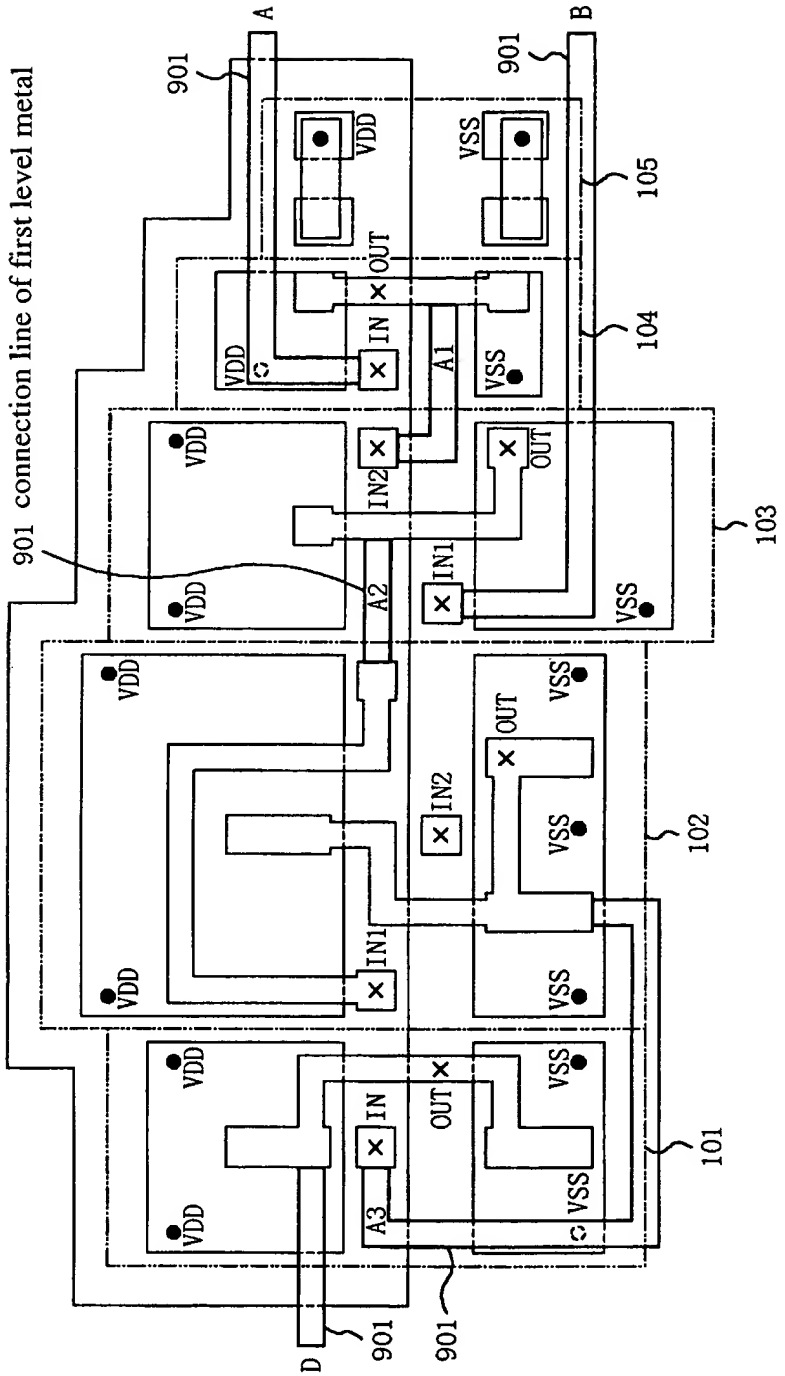
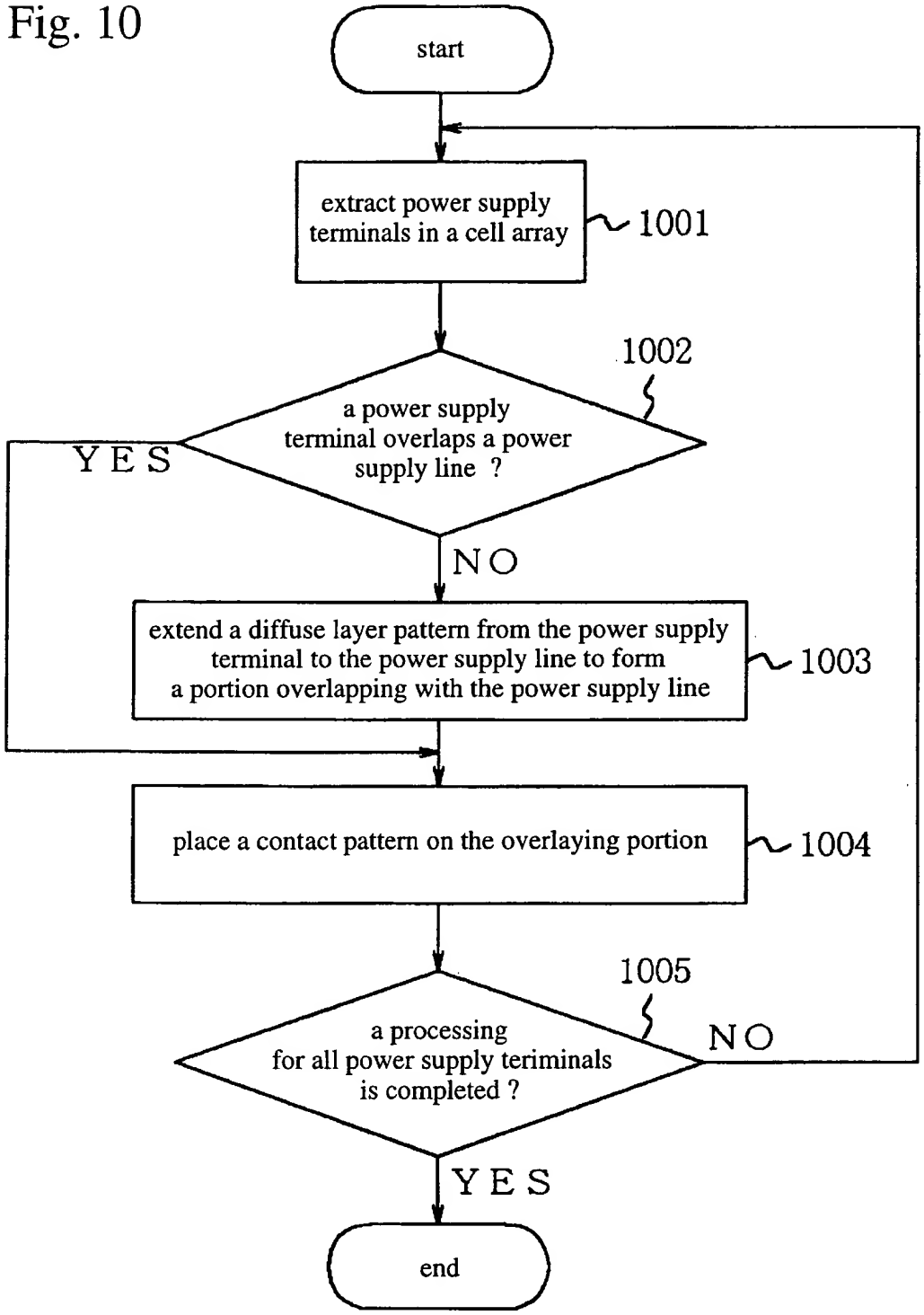

901 connection line of first level metal
A
B
C
D
901
VDD
VSS
OUT
IN
IN1
IN2
A1
A2
A3
105
104
103
102
101

Fig. 10


start
extract power supply terminals in a cell array
1001
1002
a power supply terminal overlaps a power supply line ?
YES
NO
extend a diffuse layer pattern from the power supply terminal to the power supply line to form a portion overlapping with the power supply line
1003
place a contact pattern on the overlaying portion
1004
1005
a processing for all power supply teriminals is completed ?
NO
YES
end

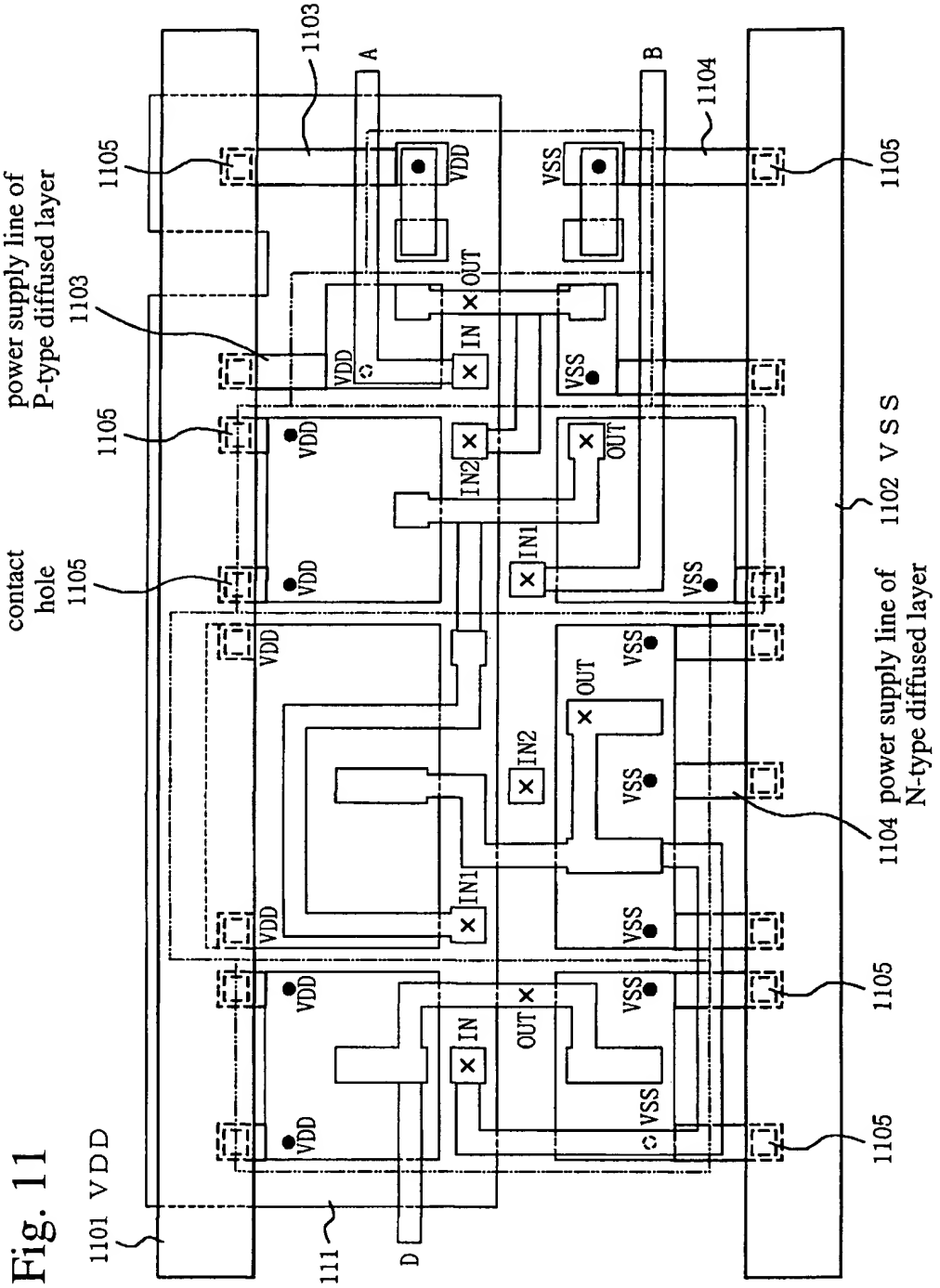

1101 VDD
1102 VSS
1103
1104 power supply line of N-type diffused layer
1105
power supply line of P-type diffused layer
contact hole
A
B
C
D
111
VDD
VSS
IN
IN1
IN2
OUT

Fig. 11

Fig. 12

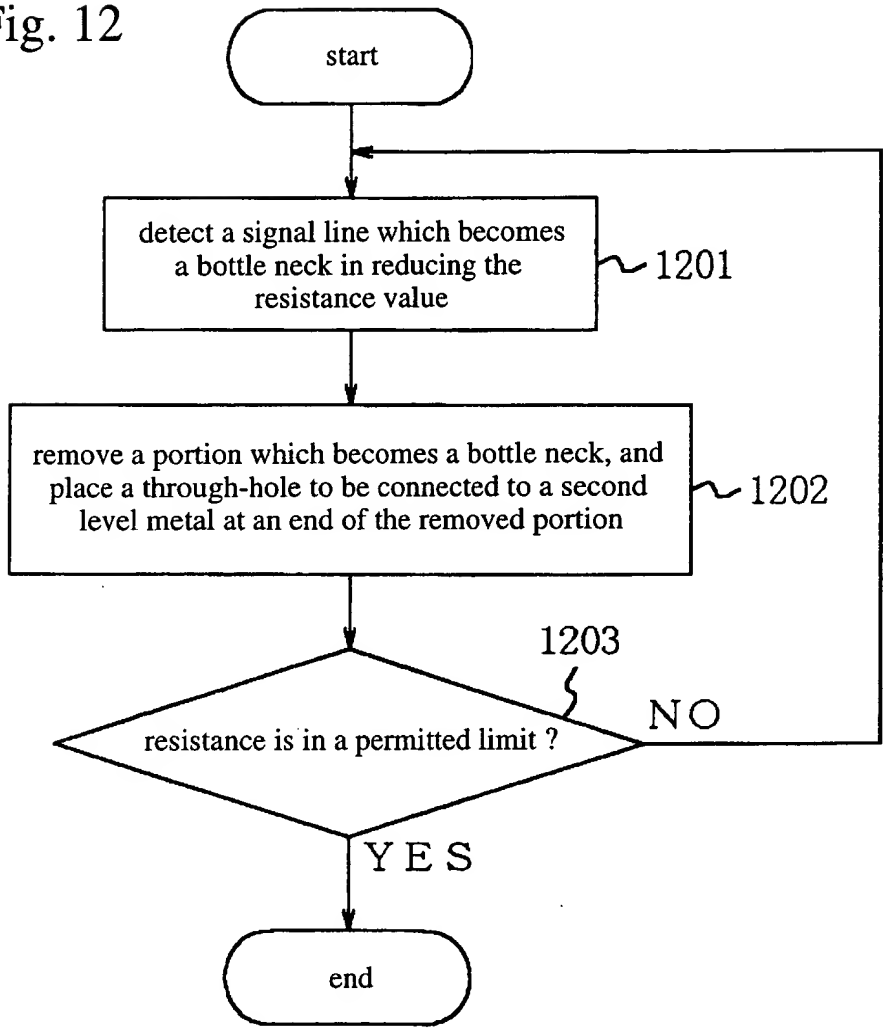
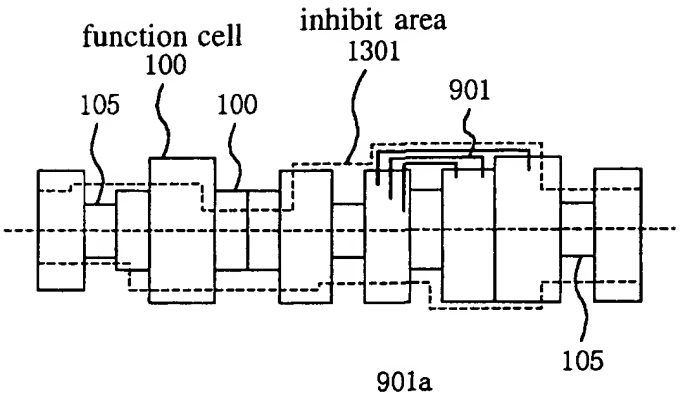
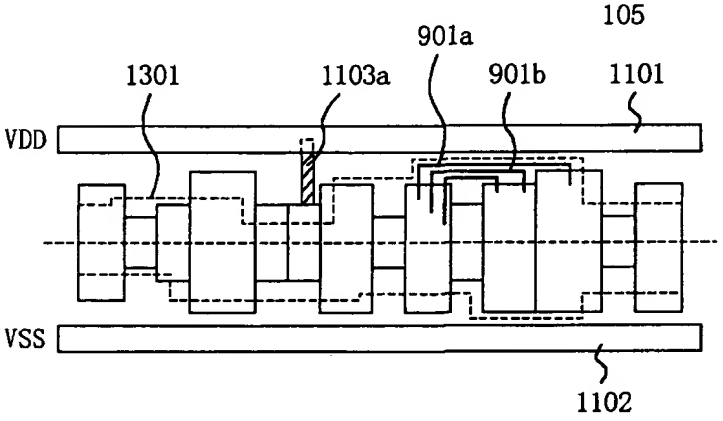

start
detect a signal line which becomes a bottle neck in reducing the resistance value
1201
remove a portion which becomes a bottle neck, and place a through-hole to be connected to a second level metal at an end of the removed portion
1202
1203
resistance is in a permitted limit ?
NO
YES
end

Fig. 13

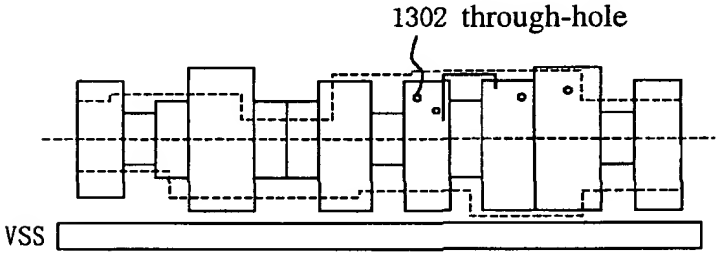
(a)


function cell
100
inhibit area
1301
105
100
901
105

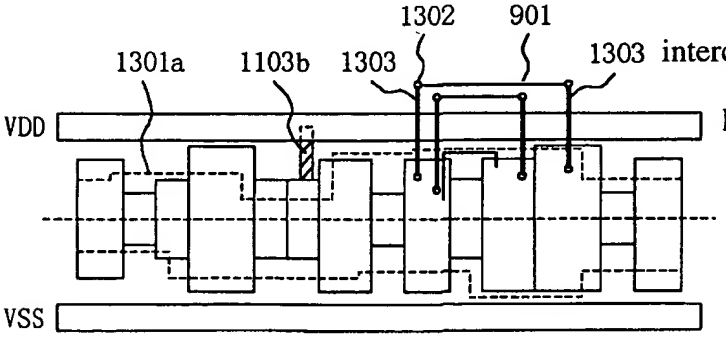
(b)


901a
1301
1103a
901b
1101
VDD
VSS
1102

(c)


1302 through-hole
VSS

(d)


1302
901
1301a
1103b
1303
1303 interconnection of second level metal
VDD
VSS

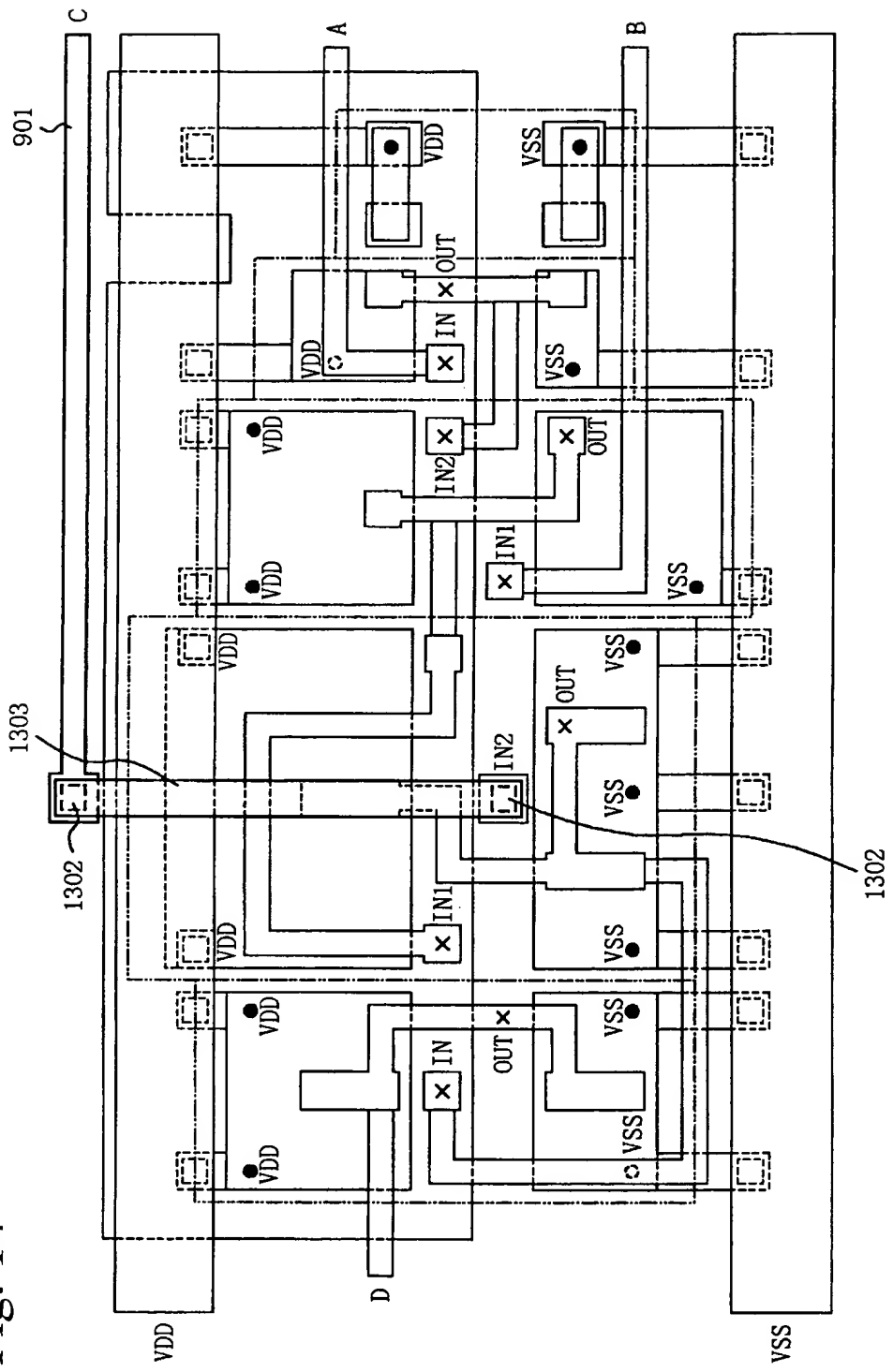


Fig. 14

Fig. 15

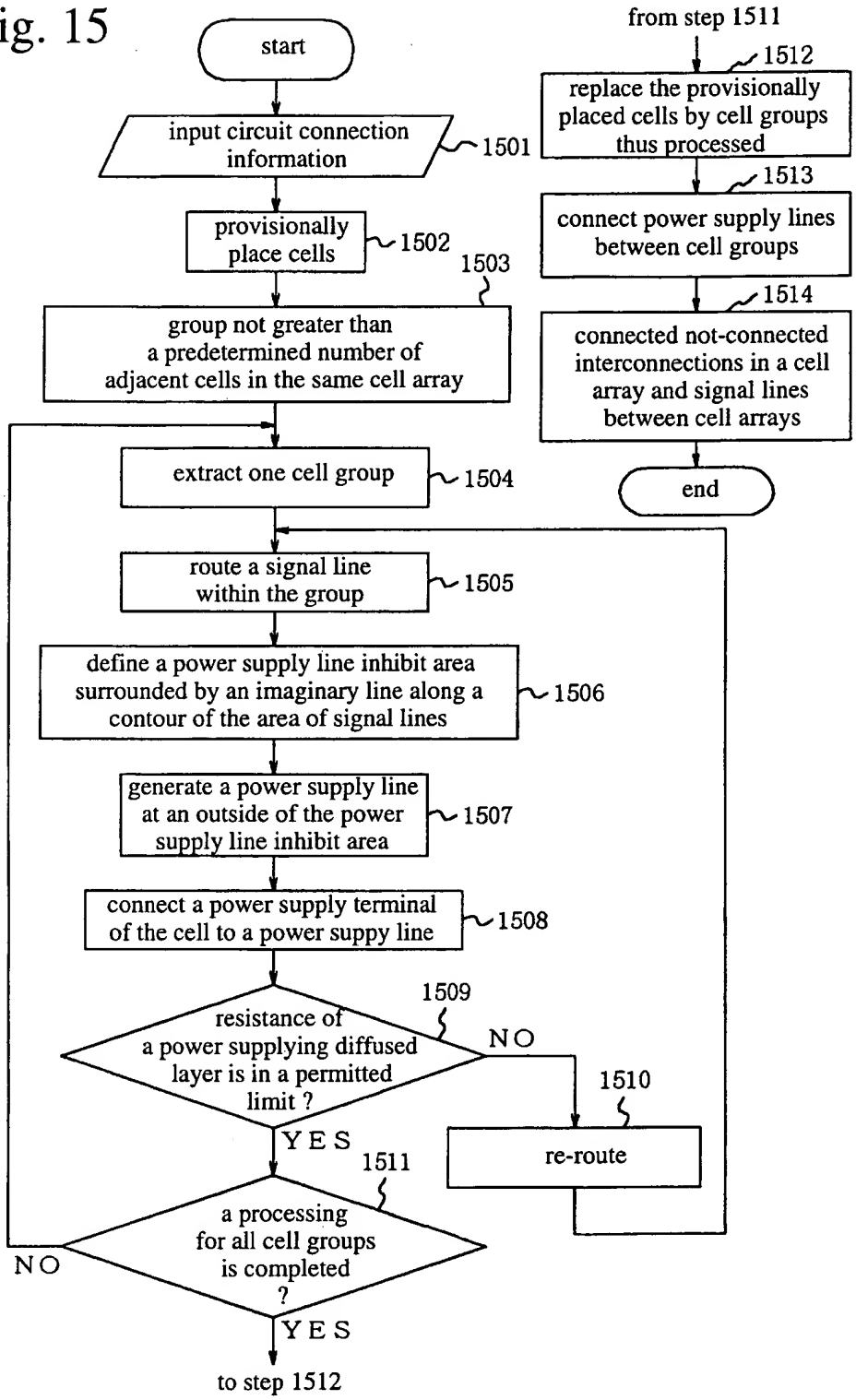
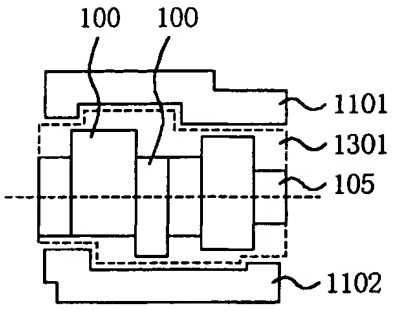
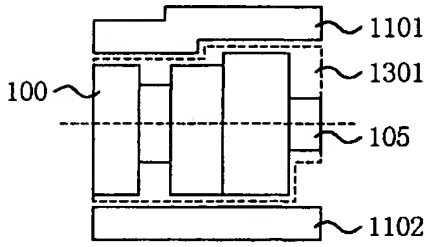

start
input circuit connection information
1501
provisionally place cells
1502
1503
group not greater than a predetermined number of adjacent cells in the same cell array
extract one cell group
1504
route a signal line within the group
1505
define a power supply line inhibit area surrounded by an imaginary line along a contour of the area of signal lines
1506
generate a power supply line at an outside of the power supply line inhibit area
1507
connect a power supply terminal of the cell to a power suppy line
1508
1509
resistance of a power supplying diffused layer is in a permitted limit ?
NO
YES
1510
re-route
1511
a processing for all cell groups is completed ?
NO
YES
to step 1512
from step 1511
1512
replace the provisionally placed cells by cell groups thus processed
1513
connect power supply lines between cell groups
1514
connected not-connected interconnections in a cell array and signal lines between cell arrays
end

Fig. 16

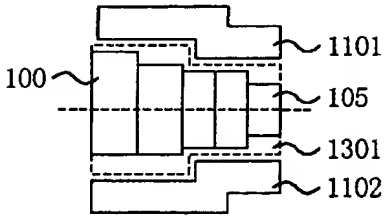
(a)


100
100
1101
1301
105
1102

(b)


1101
1301
100
105
1102

(c)


1101
100
105
1301
1102

(d)

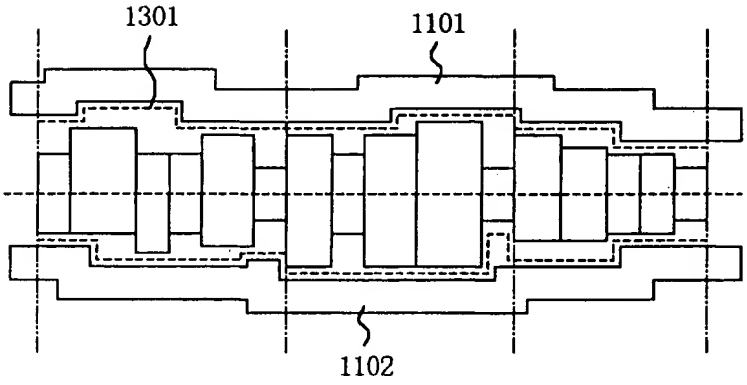

1301
1101
1102

Fig. 17

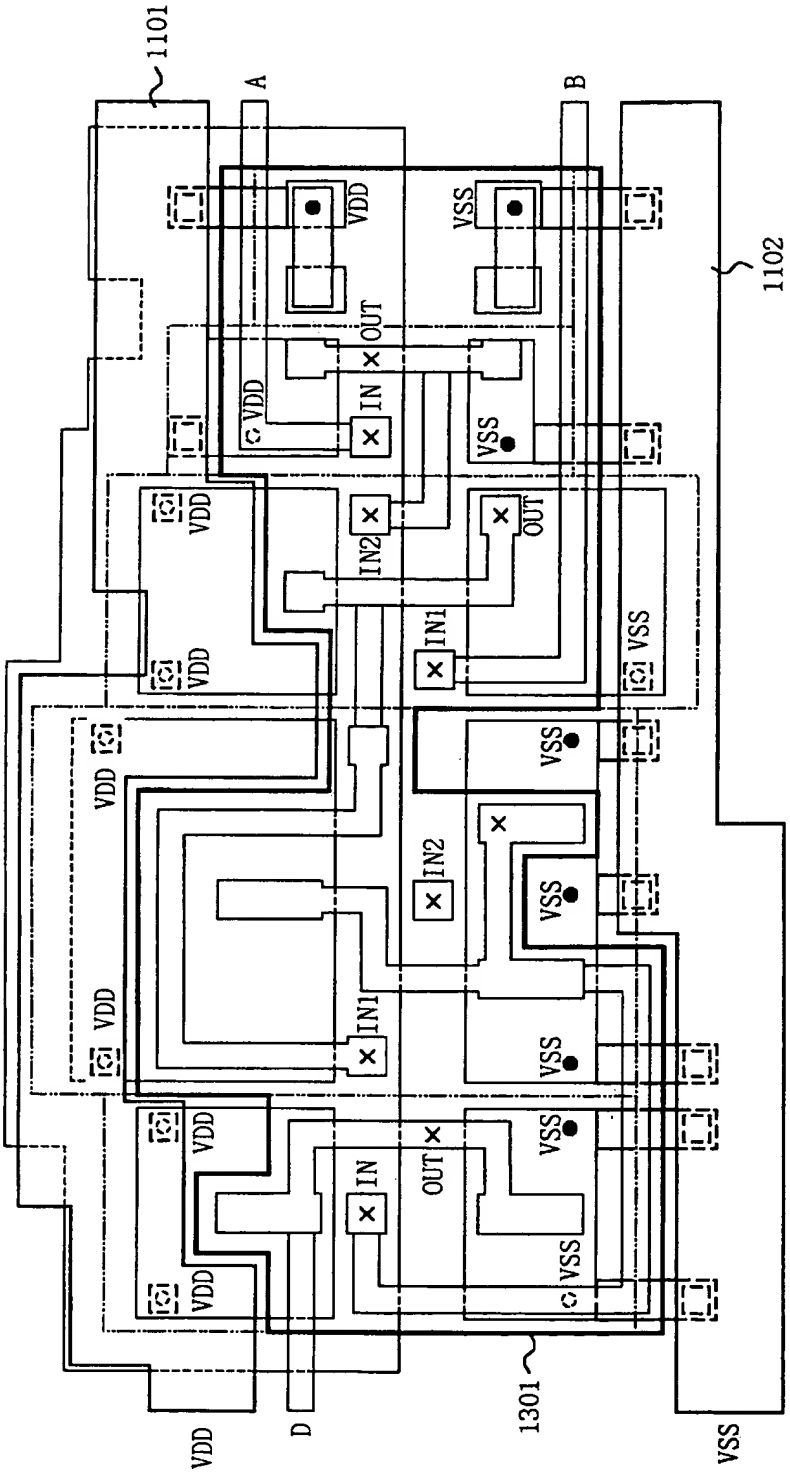
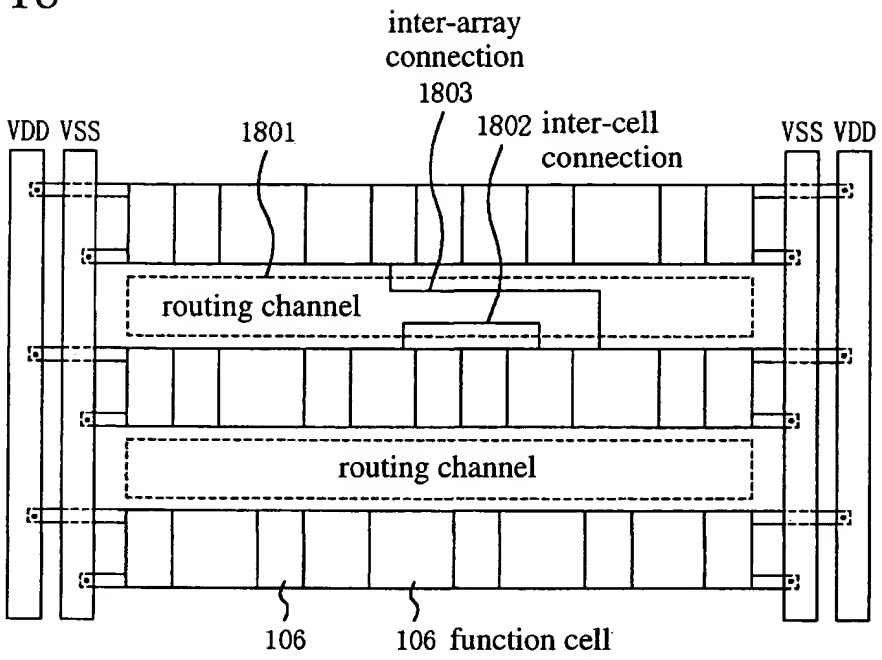


Fig. 18

(a)


inter-array
connection
1803
VDD VSS
1801
1802 inter-cell
connection
VSS VDD
routing channel
routing channel
106
106 function cell

(b)

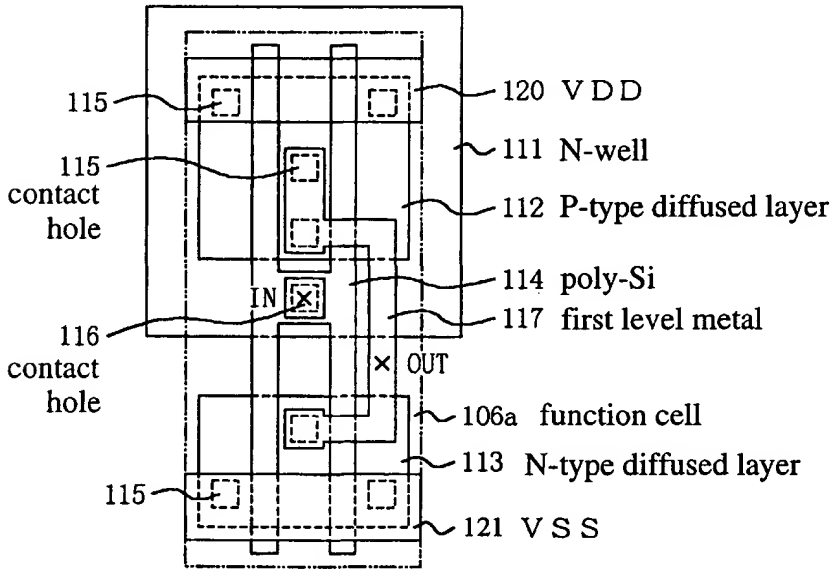
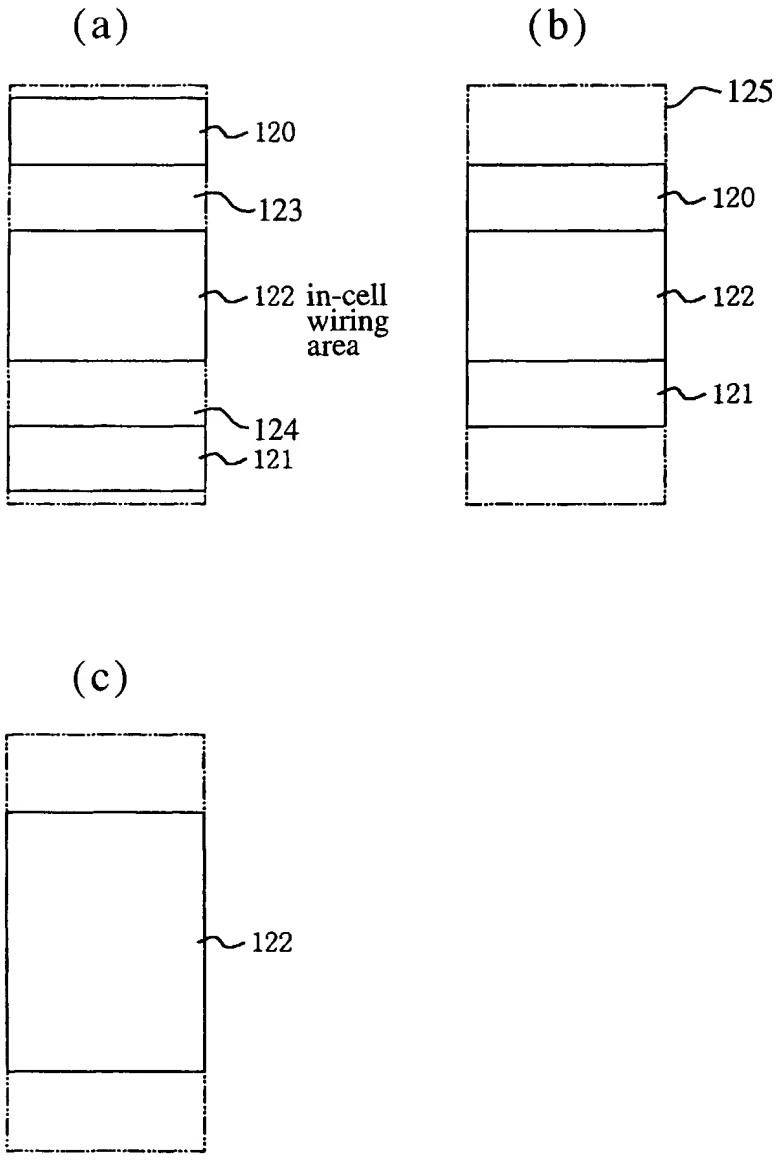

115
120 VDD
111 N-well
115
contact
hole
112 P-type diffused layer
114 poly-Si
IN
117 first level metal
116
contact
hole
OUT
106a function cell
113 N-type diffused layer
115
121 VSS

Fig. 19



[Name of Document] ABSTRACT

[Abstract]

[Object]

It is to provide a standard cell capable of forming an inter-cell connection in an area between a power supply line and an in-cell wiring area and also capable of ensuring the power supply line having an optimum line width, without a restriction requiring a constant cell width.

[Solving Means]

Standard cells each comprising a VDD power supply terminal 118 formed of a P-type diffused layer 112, a VSS power supply terminal 119 formed of an N-type diffused layer 113, and an input terminal and an output terminal formed of a first level metal 117, are used. For connecting a power supply terminal of the standard cell to a power supply line of the first level metal, a power supply line formed of the diffused layer is extended from the power supply terminal to the power supply line of the first level metal so that there is formed an overlapping portion between the power supply line of the first level metal and the power supply line formed of the diffused layer, and a contact hole is formed at the overlapping portion.

[Selected Figure] Fig. 1